1.0 REDWOOD 1 Pin List

NOTE -There are five separate and isolated VDD pins on REDWOOD 1 that can be connected to individual power sources. The number in the "GROUP" column designates which VDD power pins are used to supply power to each I/O pin. The core power pins are separate from the I/O power pins.

1.1 Clock and Reset Interface

PIN NAME	I/O	PIN DESCRIPTION	GROUP#	176PIN#	160PIN#
CLK1X2X	I	1X or 2X Clock Input: This input clock is the main system clock. This option is determined by index register 100H, bit 1. If the bit is high, the input is 2X clock; if low, it is 1X clock.	3	59	53
CPUCLKO1	O 12mA	CPU Clock Output 1: This output is always 1X clock and can be programmed to be running regardless of STOPCLK state.	1	167	153
CPUCLKO2	O 8mA	CPU Clock Output 2: It can be either 1X clock for 486 type CPU or 2X clock for 386 type CPU depending upon index register 100H, bit 1. This is the output should be connected to CPU Clock input.	1	165	151
RCRST#	I	RC-RESET #: This input is used to reset the REDWOOD 1's Power Management Controller and RTC when power is first applied to the chip.	3	56	50
PWRGOOD	I	Power Good Input: This input causes a complete system reset. It is driven low by the PWRGOOD signal from the power supply or a reset switch. On power up, PWRGOOD going from L→H indicates external VCC is stable and will wakeup the RW core from Standby →On. If PWRGOOD goes L, it will drive the chip back to Standby.	3	55	49
RSTDRV#	O 4mA	AT Bus Reset Output #: This output provides a system reset.	3	65	59
RSTCPU (RSTDRV) (RSTNPU)	O 12mA	CPU Reset Output: This is the reset output to the CPU and AT Bus. This output includes hardware generated reset only. This pin will become numeric coprocessor interface pin RSTNPU if index register 100H, bit 1 is high (386DX mode) and index register 112H, bit 14 is also high. **Note: Use SRESET for CPU with only 1 Reset Pin I/P.**	1	34	32
SPNDNRST	O 4mA	Suspend Not Reset: This output provides a reset equivalent to RSTDRV except when in Suspend Mode. Any device not powered down during Suspend Mode should use this reset.	3	67	61

1.2 CPU Interface

PIN NAME	I/O	PIN DESCRIPTION	GROUP	176PIN#	160PIN#
A<31,27:2>	I/O 4mA	CPU Addresses, A<31,27:2>: These are address inputs from the CPU/VESA local bus. They will become outputs during DMA or ISA bus master cycles.	1	172, 3:7, 9:15, 17:26, 28:31	158,1:5,7: 13, 15:24, 26:29
BE<3:0>#	I/O 4mA	CPU Byte Enables <3:0>#: These inputs control the selection of individual bytes of data. These signals become outputs during DMA or ISA bus master cycles.	1	168:171	154:157

ADS#	I/O 4mA	Address Status #: This input indicates the presence of a valid address and cycle definition from the CPU/VL Bus Master. This signal becomes an output during DMA or ISA bus master cycles.	1	155	141
RDY#	I/O 4mA	Ready #: This output to the CPU indicates completion of the current bus cycle. This pin is also an input to monitor completion of any non-system memory cycles.	1	156	142
BRDY# (PEREQO)	I/O 4mA	Burst Ready #: This output to the 486 CPU indicates completion of the current burst access. This pin is also an input to monitor the completion of local bus cycles. This pin will become numeric coprocessor interface pin PEREQO if index register 100H, bit 1 is high (386DX mode).	1	153	139
BLAST# (BUSYO#)	I/O 4mA	Burst Last #: This input from the 486 CPU indicates that the next BRDY# will complete the current burst cycle. This pin is numeric coprocessor interface pin BUSYO# if index register 100H, bit 1 is high.	1	160	146
M/IO#	I/O 4mA	Memory/IO #: This input from the CPU/VL Bus Master indicates whether the current cycle is a Memory or I/O access. This pin is an output during ISA Master or DMA mode.	1	159	145
D/C#	I/O 4mA	Data/Code #: This input from the CPU/VL Bus Master indicates whether the current cycle is a Data or Code access. This pin is an output during ISA Master or DMA mode.	1	158	144
W/R#	I/O 4mA	Write/Read #: This input from the CPU/VL Bus Master indicates whether the current cycle is a Write or Read access. This pin is an output during ISA Master or DMA mode.	1	157	143
EADS# (ERRORO#)	O 2mA	External Address Strobe #: This output to the 486 CPU indicates that a valid address has been driven onto the CPU address bus for internal cache snoop cycle. This pin will become numeric coprocessor interface pin ERROR# if index register 100H, bit 1 is high (386DX mode)	1	161	147
KEN#	O 2mA	Cache Enable #: This output to the 486 CPU indicates that the current bus cycle in cacheable.	1	40	38
HLDA	I	Hold Acknowledge: This input from the CPU indicates a Hold Acknowledge state.	1	163	149
A20M#	O 2mA	Address Bit 20 Mask #: This output to the 486 CPU indicates that the CPU should mask A20 in order to emulate the 8086 address wrap around.	1	162	148
SMIACT# (SMIADS#)	I I	System Management Interrupt Active#: This input from some CPUs indicates that an SMI routine is in progress. System Management Interrupt Address Status # : This input indicates the presentation of a valid SMI address and cycle definition on some CPU's. This function can be enabled by programming index register 103H, bit 15 high.	1	33	31
FLUSH# (IRQ13)	O 2mA	CPU Cache Flush # : This output drives the Flush# of the CPU and is used to flush CPU internal cache. This pin will become numeric coprocessor interface pin IRQ13 if index register 100H, bit 1 and index register 112H, bit 14 are high.	1	35	33
SMI# (PMI)	I/O 4mA	System Management Interrupt #: This output indicates a system management interrupt and is used to invoke the system management mode.	1	37	35
NMI (EXTACT0)	I	Non-Maskable Interrupt input : This input from REDWOOD 2 indicates a non-maskable interrupt condition. EXTACT0 input : This pin can be programmed to be EXTACT0 input if index register 112H, bit 12 is high.	1	173	159

STPCLK#	O 4mA	Stop Clock # : For some CPU's, this output indicates a stop clock request to the CPU.	1	38	36
SRESET	O 2mA	Soft Reset : This output to some CPU's indicates a software generated CPU reset request. It will be also active during a hardware generated reset condition. Note: Use this pin for CPU's with a single reset pin.	1	32	30
LOCK# (CA13) (TAGCS#) (BUSYI#)	I/O 4mA	LOCK# : This input pin from the CPU indicates the current cycle is locked. However, this is only valid when index register 100H bit 4 is low. If index register 100H, bit 4 is high, this pin becomes output mode and can be either used as CA13 (index register 110H, bit 2 high) or TAG RAM Chip Select # (index register 110H, bit 2 low) This pin is numeric coprocessor interface pin BUSYI# input if index register 100H, bit 1 is high.	1	149	135
HITM# (ERRORI#) (LOCK#)	I	HITM# : HITM# indicates the snoop cycle hits a modified line in the level 1 cache inside the CPU. This pin is numeric coprocessor interface pin ERRORI# if index register 100H, bit 1 is high. If index register 110H, bit 3 is high, this pin becomes LOCK#.	1	150	136
CACHE# (PEREQI) (PCD)	I	CACHE# : CACHE# indicates a cache operation. Together with ADS# and W/R#, they mark the beginning of a write back cycle. This pin is numeric coprocessor interface pin PEREQI if index register 100H, bit 1 is high. If index register 100H, bit 4 is low, then this pin becomes PCD from the CPU.	1	152	138
WB/WT# (SMIRDY#)	O 4mA	WriteBack / WriteThrough# : This output pin is used to define a particular line as write back or write through. It is used to mark a write protect line as write through. . System Management Interrupt Ready #: For some CPU's, this output indicates completion of a SMI bus cycle. This function will be enabled by index register 103H, bit 9 being low.	1	151	137

1.3 DRAM Interface

PIN NAME	I/O	PIN DESCRIPTION	GROUP	176PIN#	160PIN#
DRAMWE#	O 12mA	DRAM Write Enable #: This output drives Write Enable for all DRAM's.	2	93	83
RAS<2:0># (RAS<4,2,0>#)	O 12mA	Row Address Strobes <2:0>#: These outputs drive the RAS# inputs on DRAM bank pairs 2 to 0. If index register 20BH, bit 0 is high, then RAS1# becomes RAS2#, and RAS2# becomes RAS4# logically.	2	104:106	94,95,96
CAS<3:0>A#	O 12mA	Column Address Strobes <3:0># Group A: These outputs drive the CAS# inputs on DRAM bytes 3 to 0 in even banks (banks 0,2,4).	2	98, 100:102	88,90:92
CAS<3:0>B# (RAS<5,3,1>#)	O 12mA	Column Address Strobes <3:0># Group B: These outputs drive the CAS# inputs on DRAM bytes 3 to 0 in odd banks (banks 1,3,5). If index register 20BH, bit 0 is high, then CAS0B# is RAS1#, CAS1B# is RAS3#, CAS2B# is RAS5# and CAS3B# is No Connect.	2	94:97	84:87
MA0A	I/O 12mA	Memory Address 0 A: These outputs drive the MA0 line for all DRAM's in even banks.	2	121	111
MA0B	I/O 12mA	Memory Address 0 B: These outputs drive the MA0 line for all DRAM's in odd banks.	2	120	110

MA<11:1>	I/O 12mA	Memory Addresses <11:1>: These outputs drive the MA lines for all DRAM's. They are also used as RC-RESET configuration inputs during power up.	2	107:111, 113:118	97:101, 103:108
MDEN#	O 4mA	Memory Data buffer Enables : This signal is used to control the enable pins of the optional Memory Data Buffers. Use DRAMWE# as the direction control.	2	92	82

1.4 External Cache Interface

PIN NAME	I/O	PIN DESCRIPTION	GROUP	176PIN#	160PIN#
CWE<1:0>#	O 12mA	Cache Write Enable <1:0> #: Cache Data RAM Write Enables for bank 1 and bank 0.	5	130, 129	120,119
COE<1:0>#	O 12mA	Cache Output Enable <1:0># : Cache Data RAM Output Enables for bank 1 and bank 0.	1	42, 41	40,39
CCS<3:0># (3:FBE#) (2:ACPWR) (1:VLB) (0:LB)	O 4mAO I	Cache Chip Select <3:0># : Cache Data RAM Chip Selects for 4 individual bytes.These pins can also be used as FBE# output for level 2 cache control, ACPWR, VLB and LB inputs for the power management controller if index register 110H, bit 4 is high.	5	125:122	115:112
CA3A (CA3)	O 8mA	Cache Address bit 3 A : Cache Data RAM address bit 3 for odd bank when cache interleave is enabled. Or it is Cache address 3 if only one bank is used.	5	127	117
CA3B (CA2)	O 8mA	Cache Address bit 3 B : Cache Data RAM address bit 3 for even bank when cache interleave is enabled. This pin becomes Cache address 2 if only single bank of SRAM is used.	5	128	118
TAGD<7:0> (7:HIT#) (6:PC9) (5:PC8) (4:PC7) (3:PC6) (2:PC5) (1:PC4) (0:Reserved)	I/O 4mA	TAG Data <7:0> : TAG RAM Data bits. In a non-cached system or a system with external TAG comparator chip, these pins can be used as addtional PC's (power control pins) as defined by index register 110H, bit 5 being high. TAGD7 is HIT# signal from the external TAG comparator. TAGD<6:1> are PC<9:4>. (See section 1.6 Power Management Interface for detailed descriptions for these pins).	5	136:139, 141:144	122:125, 127:130
TAGWE#	O 4mA	TAG RAM Write Enable # : TAG Data Write Enable is the write strobe to the TAG RAM.	5	135	121
DIRTY (WAKE0) (GPIOB0)	I/O 4mA	DIRTY bit : Dirty bit indicates the particular line in the level 2 cache contains modified data.If index register 111H, bit 4 is high and bit 5 is low, then this pin is redefined as WAKE0 input for the wake control logic. Furthermore, if index register 111H, bits 4 and 5 are high, then this pin can be used as a general purpose IO (GPIOB0). Use index register 014H, bits 4 and 6 to control the function of GPIOB0.	5	146	132
DRTWE# (WAKE1) (GPIOB1) (NMI)	I/O 4mA	DiRTy bit Write Enable # : Dirty bit Write Enable is the write strobe to the Dirty RAM.If index register 111H, bits 3 and 6 are high and bit 7 is low, then this pin is redefined as WAKE1 input for the wake control logic. Furthermore, if index register 111H, bits 3, 6 and 7 are all high, then this pin can be used as a general purpose IO (GPIOB1). Use index register 014H, bits 5 and 7 to control the function of GPIOB1. This pin can also be used as NMI input if index 111H, bit 6 is high and bit 3 is low.	1	147	133

SRAMCE#	O 4mA	SRAM Chip Enable # : This pin will be used to enable the data RAM's. It will be used in conjunction with CCS<3:0># to control the SRAM's. This pin is needed in the system using 64Kx16 RAM's.	1	174	160

1.5 AT Bus Interface and Miscellaneous Controls

PIN NAME	I/O	PIN DESCRIPTION	GROUP	176PIN#	160PIN#
MASTER#	I	Master #: This input from the AT Bus indicates that a slot Master has taken control of the AT Bus.	3	54	48
KBCS#	O 2mA	KeyBoard controller Chip Select #: This output drives the 8042, or equivalent, Keyboard Controller Chip Select.	3	68	62
ROMCS#	O 2mA	ROM Chip Select #: This output drives the BIOS ROM Chip Select.	3	69	63
IRQ8#	I/O 2mA	IRQ 8 # output from the internal RTC. It will become an input if index register 100H, bit 11 is high (external RTC mode).	3	70	64
KBRST# (GPIOC1) (GPCS0#)	I/O 4mA	KeyBoard controller CPU ReSet #: This pin can be connected to the keyboard controller as the indication of a keyboard controller initiated CPU reset condition if index register 111H, bit 8 is low. If index register 111H, bits 8/9/10 are high and bit 11 is low, then this pin can be used as a general purpose IO pin (GPIOC1). Use index register 014H, bits 11 and 9 to control the function of GPIOC1. If index register 111H, bits 8, 9 10 and 11 are high, then this pin can be used as a General Purpose Chip Select (GPCS0#).	3	66	60

1.6 Power Management Interface

PIN NAME	I/O	PIN DESCRIPTION	GROUP	176PIN#	160PIN#
32KIN	I	32KHZ Input: This input is used for the internal RTC block and power management circuit.	3	57	51
PC<0>	O 2mA	Power Controls <0>: This pin provides power control for one system component or power plane.	3	61	55
PC<1>	O 2mA	Power Controls <1>: This pin provides power control for one system component or power plane.	3	62	56
PC<2> (GPIOC0) (GPCS1#)	I/O 2mA	Power Controls <2>: This output provide individual power control for any system component. If index register 110H, bit 8 is low (both 112H, bit 2 and 110H, bit 7 are high), then this pin can be used as a general purpose IO pin (GPIOC0). Use index register 014H, bits 10 and 8 to control the function of GPIOC0. If index register 110H, bit 8 is also high (both 112H, bit 2 and 110H, bit 7 are high), then this pin is a General Purpose Chip Select (GPCS1#)	3	63	57

PC<3> (GPCS2#) (HTRGOUT)	O 2mA	Power Controls <3>: This output provide individual power control for any system component. If index register 112H, bit 3 and 110H, bit 9 are high, 110H, bit 10 is low, then this pin can be used as a General Purpose Chip Select (GPCS2#)Heat Regulator Output: This output can optionally be enabled to indicate the output function of the internal Heat Regulator. This function can be enabled by programming both 112H, bit 3 and 110H, bits 9 and 10 high.	3	64	58
GPIO<3:0> (3:EXTACT1) (2:RING) (2:MDEN#) (1:KBGA20) (1:KBCLKO) (0:FRCSLW) (0:GPEXT) (2: ASRTC, 1: DSRTC, 0:RWRTC)	I/O 4mA	General Purpose I/O's <3:0>: These four I/O's are provided for general purpose usage. This pin can also be selected as the EXTACT1 input. This pin can also be used as the RING input from the modem if index register 111H, bit 14 is high and 100H, bit 0 is low. This pin can also be used as the MDEN# output for the MD buffer control if index register 111H, bit 14 and 100H, bit 0 are both high. This pin can also be used as the input for KB controller GateA20 function if index register 111H, bit 13 is high and 112H, bit 13 is low. This pin can also be the KB Clock output if index register 111H, bit 13 and 112H, bit 13 are both high. FRCSLW/GPEXT: This pin may be used as Force Slow input or GPEXT ouput by programming index register 111H, bits 0 and 12.If index register 111H, bit 12 is high and bit 0 is low, then it is FRCSLW input. If both bits are high, then it is GPEXT ouput If index register 100H, bit 11 is high, an external RTC chip is used. This condition will overwrite other configuration bits and GPIO<2:0> will provide interface signals to the external RTC : GPIO2 = ASRTC, GPIO1 = DSRTC and GPIO0 = RWRTC.	3	53:50	47:44
SWTCH	I	Switch: This input provides an on-off function between Fully-On and Suspend or Standby Modes.	3	47	41

1.7 Battery Management Interface

PIN NAME	I/O	PIN DESCRIPTION	GROUP
ACPWR	I	AC Power: This input indicates that the power source is AC. **Note: This pin is multiplexed with CCS2#. Using index register 110H, bit 4 to select between CCS2# and AC Power Function.**	5
VLB	I	Very Low Battery: This input from the power supply indicates a very low battery condition. **Note: This pin is multiplexed with CCS1#. Using index register 110H, bit 4 to select between CCS1# and Very Low Battery Function.**	5
LB	I	Low Battery: This input from the power supply indicates a low battery condition. **Note: This pin is multiplexed with CCS0#. Using index register 110H, bit 4 to select between CCS0# and Low Battery Function.**	5

1.8 Burst Bus Interface

PIN NAME	I/O	PIN DESCRIPTION	GROUP	176PIN#	160PIN#
BADS#	I/O 4mA	Burst Bus ADS# : This is the signal used to indicate the various phases of the burst bus (including the status phase, address phase, data transfer phase and miscellaneous information phase).	4	81	75
FS1XCLK	O 8mA	Fast 1X Clock : This is the fast version of the 1X clock. It can be either the divided CPU clock or the undivided input clock.	4	80	74
BD<7:0>	I/O 4mA	Burst Data Bus <7:0> : This 8-bit bus carries different information during various phases.	4	71:78	65:72
BDEV#	I/O 4mA	Burst Device # : This is the signal all the devices on the burst bus can use to claim burst bus cycle. This signal is also used as READY indicator to terminate or extend the burst bus cycle.	4	82	76
BSER	I	Burst Serial Bus : This pin is used between REDWOOD 1 and REDWOOD 2 to indicate various activities for power management circuit.	4	83	77

1.9 Power and Ground Pins

PIN NAME	I/O	PIN DESCRIPTION	GROUP	176PIN#	160PIN#
VDDCL<1:0>	–	Core Logic Power Pins	–	39, 148	37,134
VDDIO1	–	I/O Power Pins for Group 1	1	16, 36, 164	14,34, 150
VDDIO2	–	I/O Power Pins for Group 2	2	99, 112	89,102
VDDIO3	–	I/O Power Pins for Group 3	3	58	52
VDDIO4	–	I/O Power Pins for Group 4	4	79	73
VDDIO5	–	I/O Power Pins for Group 5	5	126, 145	116,131
VSSIO<11:0>	–	I/O Ground Pins	–	8, 27, 48, 49, 60, 84, 85, 85, 103, 119, 140, 154, 166	6,25, 42,43,54, 78,79,93, 109,126, 140,152

1.10 Multi-Function NPU Pins

The interface control signals between a 386DX and a 387 NPU are significantly different from those used in a 486 system. In order to save pins, the signals that are unique to the 386 implementation are shared with signals that are unique to the 486. The following table indicates which pins are shared and describes the 386 function of each.

Multi-function Pins -- 486 vs 386DX

486 NAME	386 NAME	I/O	386 DESCRIPTION	PAD I/O	176PIN#	160PIN#
EADS#	ERRORO#	O	Error output #: This pin is the modified ERROR output to the 386DX.	O	161	147
CACHE#	PEREQI	I	Processor Extension Request Input: This input from a 387 indicates an NPU cycle request.	I	152	138
BRDY#	PEREQO	O	Processor Extension Request Output: This output to a 386DX indicates an NPU cycle request.	I/O	153	139
HITM#	ERRORI#	I	Error Input #: This pin is the ERROR input from a 387 NPU.	I	150	136
BLAST#	BUSYO#	O	Busy Output # : This output to a 386DX indicates that the NPU is executing NPU cycles.	I/O	160	146
RSTCPU	RSTNPU	O	Reset NPU: This output signals a reset for the 387 NPU.	O	34	32
LOCK#	BUSYI#	I	Busy Input # : This input from the a 387 NPU indicates that it is executing NPU cycles.	I/O	149	135
FLUSH#	IRQ13	O	IRQ13 output : This output is used by the 387 handler to cause an numeric coprocessor interrupt.	O	35	33

2.0 REDWOOD 2 Pin List

NOTE -There are three separate and isolated VDD pins on REDWOOD 2 that can be connected to individual power sources. The number in the "GROUP" column designates which VDD power pins are used to supply power to each I/O pin. The core power pins are separate from the I/O power pins.

2.1 Clock and Reset Interface

PIN NAME	I/O	PIN DESCRIPTION	GROUP	176PIN#	160PIN#
14MHZIN	I	14.318 MHz Input: This input is used to generate the timer clock for the 82C206 Peripheral Controller.	3	137	123
CPUCLK	I	CPU Clock Input : This will be the 1X clock input from REDWOOD1 (It should be connected CPUCLKO1). If index register 100H, bit 1 is high (386DX mode), this clock will be half of the CPU frequency.	1	157	143
RSTDRV#	I	Reset # Input: This is the master Reset pin for REDWOOD 2. This is an active low signal.	3	119	109

2.2 CPU Interface

PIN NAME	I/O	PIN DESCRIPTION	GROUP	176PIN#	160PIN#
D<31:0>	I/O 4mA	CPU Data <31:0>	1	40:36, 34:25, 23:14, 12:9, 7:5	38:34, 32:23, 21:12, 10:7,5:3
RDY#	I/O 4mA	Ready #: This output to the CPU indicates completion of the current bus cycle. This pin is also an input to monitor completion of local bus cycles.	1	172	158
BRDY#	I	Burst Ready #: This input allows REDWOOD 2 to monitor the CPU burst cycle activity.	1	171	157
DP<3:0> GPIO<7:4>	I/O 4mA	Data Parity <3 :0> These pins can also be selected as additional General Purpose IO pins. Their function can be enabled by index register 302H, bits <1:0> and controlled by index register 304H, bits<15:8>.	1	167:170	153:156
FERR# (W/R#)	I	Floating Point Error #: This input from the 486DX CPU indicates a 486DX internal floating point error. This pin can also be programmed to be CPU W/R# status for parity generation circuit by index register 302H, bit 12 high.	1	166	152
IGNNE#	O 2mA	Ignore Numeric Error #: This output to the 486DX CPU indicates that floating point errors should be ignored.	1	165	151
INTR	O 2mA	CPU Interrupt Request from the 8259A Interrupt Controller.	1	163	149
HOLD	O 2mA	Hold Request: This output to the CPU indicates a request to hold the CPU and float its bus.	1	162	148
HLDA	I	Hold Acknowledge: This input from the CPU acknowledges a Hold Request.	1	161	147

NMI	O 2mA	Non Maskable Interrupt: This output to the CPU indicates the occurrence of a Non Maskable Interrupt.	1	160	146
HITM# (IRQ13)	I	HITM# : HITM# indicates that the snoop cycle hits a modified line in level 1 cache. REDWOOD2 uses it to decide if it needs to back off from a HOLD REQUEST cycle. IRQ13: This pin can be used as IRQ13 input for the numeric coprocessor if index register 302H, bit 12 is high.	1	159	145

2.3 VESA Bus Interface

PIN NAME	I/O	PIN DESCRIPTION	GROUP	176PIN#	160PIN#
LOCAL#	I	Local Device #: This input from a local bus device indicates that the local device has claimed the current CPU cycle and REDWOOD 2 should not start any ISA bus or Burst bus cycle..	1	158	144
LRDY#	I	Local Device READY# : This signal indicates the local device has completed the cycle.	1	41	39
LREQ1# (LOCAL2#)	I	Local bus master Request1# : VESA Bus Request input from one of the two bus master devices. LOCAL2# : This pin can also become the third LDEV# input from the VL bus. This is done by programming index register 302H, bit 5 high.	1	173	159
LREQ0#	I	Local bus master Request0# : VESA Bus Request input from one of the two bus master devices.	1	3	1
LGNT1# (LOCAL1#)	I/O 2mA	Local bus master Grant1# : VESA Bus Grant outputs to the bus master devices indicating which bus master can own the bus. LOCAL1# : This pin can also become the second LDEV# input from the VL bus. This is done by programming index register 302H, bit 5 high.	1	174	160
LGNT0#	O 2mA	Local bus master Grant0# : VESA Bus Grant outputs to the bus master devices indicating which bus master can own the bus.	1	4	2

2.4 AT Bus Interface

PIN NAME	I/O	PIN DESCRIPTION	GROUP	176PIN#	160PIN#
SA<1:0>	I/O 12mA	Slot Addresses <1:0>: These outputs are decoded from the CPU byte enables to drive these AT Bus address lines.	3	109, 108	99,98
SBHE#	I/O 12mA	Slot Byte High Enable #: This output to the AT Bus indicates a data transfer on the high byte of the Slot Data Bus.	3	110	100
SD<7:0>	I/O 12mA	Slot Low Byte Data <7:0>: These I/O are the data read and write path for the AT Bus.	3	61:58, 57:53	55:53, 51:47
SD<15:8> (MSA<7:0>)	I/O 12mA	Slot High Byte Data <15:8>: These I/O are the data read and write path for the AT Bus. They will also drive the refresh address SA<7:0> during AT refresh cycles if index register 302H, bit 8 is programmed to high.	3	70, 68:62	64, 62:56
BALE	O 12mA	Buffered Address Latch Enable: This output is driven to the AT Bus where it indicates the presence of a valid address on the Bus.	3	123	113
MASTER#	I	Master #: This input from the AT Bus indicates that a slot Master has taken control of the AT Bus.	3	116	106

MEMR#	I/O 12mA	Memory Read #: This output to the AT Bus indicates a Memory Read cycle to any valid AT Bus address. This pin also acts as an input to provide for MASTER access to local DRAM.	3	113	103
MEMW#	I/O 12mA	Memory Write #: This output to the AT Bus indicates a Memory Write cycle to any valid AT Bus address. This pin also acts as an input to provide for MASTER access to local DRAM.	3	114	104
SMEMR#	O 12mA	Slot Memory Read #: This output to the AT Bus indicates a Memory Read cycle within the 0 to 1MB address range.	3	49	43
SMEMW#	O 12mA	Slot Memory Write #: This output to the AT Bus indicates a Memory Write cycle within the 0 to 1MB address range.	3	48	42
IOR#	I/O 12mA	I/O Read #: This output to the AT Bus indicates an I/O Read cycle.	3	51	45
IOW#	I/O 12mA	I/O Write #: This output to the AT Bus indicates an I/O Write cycle.	3	50	44
MEMCS16#	I	Memory Chip Select 16 Bit #: This input from the AT Bus indicates that the current access is to a 16 bit memory device.	3	111	101
IOCS16#	I	I/O Chip Select 16 Bit #: This input from the AT Bus indicates that the current access is to a 16 bit I/O device.	3	124	114
IOCHCK#	I	I/O Channel Check #: This input indicates a parity error from some device on the AT Bus.	3	117	107
IOCHRDY	I	I/O Channel Ready: When this input is driven low it indicates that the device on AT Bus currently being accessed requires additional time to complete the cycle.	3	118	108
ZWS#	I	Zero Wait State #: This input from the AT Bus indicates that the device currently being accessed can complete the cycle with zero wait states.	3	120	110
SYSCLK	O 12mA	System Clock: This output to the AT Bus provides an approximate 8MHZ clock.	3	122	112
AEN	O 12mA	Address Enable: This output to the AT Bus indicates that the DMA controller has taken control of the CPU address bus and the AT Bus command lines.	3	115	105
TC	O 12mA	Terminal Count : Signal on the ISA bus indicating a terminal count has reached for a given channel.	3	84	78
REFRESH#	I/O 12mA	Refresh #: This output drives the AT Bus to indicate a Memory Refresh Cycle.	3	121	111
IRQ<15:14>	I	Interrupt Request <15:14> Inputs : These are the ISA interrupt request lines.	3	107, 106	97,96
IRQ<12:3>	I	Interrupt Request <12:3> Inputs : These are the ISA interrupt request lines. Note : IRQ8 should be connected to IRQ8# of R1 or the external RTC.	3	105, 104, 102:95	95:94, 92:85
IRQ<1>	I	Interrupt Request 1 Input : These are the ISA interrupt request lines.	3	94	84
DRQ<2:0>	I	DMA Channel <2:0> Requests : AT DMA channels <2:0> request inputs.	3	76, 73, 71	70,67,65
DRQ< 3>	I/O 4mA	DMA Channel 3 Request : AT DMA channel 3 request input.	3	79	73
DRQ<7:5>	I/O 4mA	DMA Channel <7:5> Requests : AT DMA channels <7:5> request inputs.	3	83, 82, 80	77,76,74
DACK<3:0>#	O 4mA	DMA Acknowledge <3:0> outputs : Each DACK output represents the corresponding DMA channel acknowledge.	3	85, 77, 75, 72	79,71,69,66
DACK<7:5>#	O 4mA	DMA Acknowledge <7:5> outputs : Each DACK output represents the corresponding DMA channel acknowledge.	3	92, 91, 86	82,81,80

2.5 Buffer Control

PIN NAME	I/O	PIN DESCRIPTION	GROUP	176PIN#	160PIN#
XDDIR	O 2mA	XD buffer DIRection control : This pin is used to control the direction of the optional buffer between XD<7:0> and SD<7:0>.	3	42	40
SAEN# (TYPE2)	O 2mAI	SA buffer ENable# : This pin is the enable signal for the optional buffer between CPU address bus and SA bus. (The direction will be controlled by MASTER#). This pin will be used as an input to select between a 160 Pin package and 144 Pin package. If it is high at RESET, the package type is 160 pins. If it is low, then it is 144 pins.	3	127	117

2.6 Burst Bus Interface

PIN NAME	I/O	PIN DESCRIPTION	GROUP	176PIN#	160PIN#
BADS#	I/O 4mA	Burst Bus ADS# : This is the signal used to indicate the various phases of the burst bus (including the status phase, address phase, data transfer phase and miscellaneous information phase).	4	144	130
FS1XCLK	I	Fast 1X Clock : This is the fast version of the 1X clock.	4	146	132
BD<7:0>	I/O 4mA	Burst Data Bus <7:0> : This 8-bit bus carries different information during various phases.	4	148:155	134:141
BDEV#	I/O 4mA	Burst Device # : This is the signal all the devices on the burst bus can use to claim burst bus cycle. This signal is also used as READY indicator to terminate or extend the burst bus cycle.	4	143	129
BSER	O 2mA	Burst Serial Bus : This pin is used between REDWOOD 1 and REDWOOD 2 to indicate various activities for power management circuit.	4	141	127
BINT#	I	Burst Bus Interrupt # : This pin is used to indicate an interrupt request has happened on the burst bus.	4	142	128

2.7 Miscellaneous Control Signals

PIN NAME	I/O	PIN DESCRIPTION	GROUP	176PIN#	160PIN#
SPKR	O 2mA	Speaker Data Output : This pin drives the system speaker.	3	139	125
TURBO	I/O 4mA	TURBO bus enable : This signal is used to isolate the commands for the IDE drives from ordinary ISA devices.	3	126	116
DETURBO	I/O 4mA	DETURBO function : This pin is connected to the DETURBO toggle switch. Whenever this button is pressed, the system will toggle between "Normal" mode and "DETURBO" mode".	3	140	126
IDECS0#	O 8mA	IDE Chip Select 0 : This output is active when the hard drive registers from 1F0H-1F7H are selected if the primary address is used or when 170H-177H are selected if the secondary address is used.	3	129	119
IDECS1#	O 8mA	IDE Chip Select 1 : This output is active when the hard drive registers from 3F6H-3F7H are selected if the primary address is used or when 376H-377H are selected if the secondary address is used.	3	130	120

IDED7	I/O 4mA	IDE Data bit 7 : This pin provides data bit 7 to the IDE drive during the accesses in the address range 1F0H-1F7H, 170H-177H and 3F6H/376H. This pin is tri-stated during reading or writing addresses 3F7H and 377H.	3	135	121
IDEBUFEN#	O 4mA	IDE Buffer Enable # : This pin controls the external data buffers between the IDE drive(s) and SD bus.	3	136	122

2.8 Power and Ground Pins

PIN NAME	I/O	PIN DESCRIPTION	GROUP	176PIN#	160PIN#
VDDCL<1:0>	–	Core Logic Power Pins	–	78, 138	72,124
VDDIO1	–	I/O Power Pins for Group 1	1	13, 35	11,33
VDDIO3	–	I/O Power Pins for Group 3	3	47, 74, 103, 125	41,68,93,115
VDDIO4	–	I/O Power Pins for Group 4	4	147	133
VSSIO<11:0>	–	I/O Ground Pins		8, 24, 52, 58, 69, 81, 93, 112, 145, 156	6,22,46, 52,63,75, 83,102, 131,142

3.0 Configuration Register Specifications

3.1 Configuration Index and Data Ports

All REDWOOD Configuration Registers are indexed at address 24H and all data are accessed at address 26H. Also note that all registers are word width and must be accessed as such -- they cannot be accessed by byte commands. Default values for all registers are indicated each registers description. Some bits are listed as reserved these should never be changed from their default values.

3.2 Power-On Configuration

REDWOOD incorporates a power-on Configuration Register to define several fundamental system configuration variables that must be set by hardware options. It also defines several bits as miscellaneous configuration bits that may be used in conjuction with a simple BIOS routine to control system variables by jumper option. These may be defined by the system designer to control any function he desires.

The power-on register is loaded on the leading edge of the POWERGOOD pulse. This pulse should be triggered by power first being applied to the REDWOOD. At this time the present value of the memory address pins MA<11:0> will be loaded into the corresponding register bits of the power-on Register. Once set this register becomes read-only. In order to select the desired options for a particular system, each MA pin should have either a pull-up or pull-down connected. From the point of powering up the REDWOOD until slightly past the leading edge of the POWERGOOD pulse all MA pins will be floating. Thereby the pull-up or pull-down will easily set each MA pin to the appropriate high or low value. 100K resistors are recommended.

Please note that the MA pins have no internal pull-downs. Thereby every MA pin must have either a pull-up or pull-down connected externally to ensure proper Power-On sampling.

4.0 REDWOOD 1 Register Specifications

4.1 System Register Specifications

4.1.0 Power-On Register		Configuration Index 100H	
BIT	NAME	FUNCTION	DFLT
0	FIRSEL	REDWOOD/FIR Select : If low, the chip is packaged as REDWOOD (160 pin package). If high, then it is in 144 pin package as FIR. This bit is sampled from MA0A on power-up and is otherwise read only.	0
1	386SEL	386 Select: High selects the 386 CPU, low selects the 486. This bit is sampled from MA1 on power-up and is otherwise read only.	0
2	Reserved	This bit is sampled from MA2 on power-up and is otherwise read only	0
3	Reserved	This bit is sampled from MA3 on power-up and is otherwise read only	1
4	CPUMODESEL	CPU Mode Select: High selects CPU with L1 WB cache, low selects the other CPU types. This bit is sampled from MA4 on power-up and is otherwise read only.	0
5	Reserved	This bit is sampled from MA5 on power-up and is otherwise read only	0
6	Reserved	This bit is sampled from MA6 on power-up and is otherwise read only	1
9:7	Reserved	This bit is sampled from MA<9:7> on power-up and is otherwise read only	000
10	Reserved	This bit is sampled from MA10 on power-up and is otherwise read only	0
11	EXTRTC	Optional External RTC: When high, it indicates an external RTC chip is used in the system and 3 GPIO pins will be used to interface to it. Otherwise, use the internal RTC. This bit is sampled from MA11 on power-up and is otherwise read only.	0
12	Reserved	This bit is sampled from MA0B on power-up and is otherwise read only	0
15:13	Reserved		XXX

4.1.1 Non-Cacheable Region 1 Register		Configuration Index 101H	
BIT	NAME	FUNCTION	DFLT
0	NCR1EN	Enable Non-Cacheable Region 1: 1 = enabled; 0 = disabled.	0
2:1	NCR1BS<1:0>	Non-Cacheable Region 1 Block Size: Bits<2:1> — Block Size 0H — 32KB 1H — 64KB 2H — 128KB 3H — 256KB	0H
15:3	NCR1A<27:15>	Non-Cacheable Region 1 Starting Address: The Non-Cacheable Region starting address must be a multiple of the block size.	000H

4.1.2 Non-Cacheable Region 2 Register		Configuration Index 102H	
BIT	NAME	FUNCTION	DFLT
0	NCR2EN	Enable Non-Cacheable Region 2: 1 = enabled; 0 = disabled.	0
2:1	NCR2BS<1:0>	Non-Cacheable Region 2 Block Size: Bits<2:1> Block Size 0H 32KB 1H 64KB 2H 128KB 3H 256KB	0H
15:3	NCR2A<27:15>	Non-Cacheable Region 2 Starting Address: The non-cacheable region starting address must be a multiple of the block size.	000H

4.1.3 SYS Miscellaneous Control Register 1		Configuration Index 103H	
BIT	NAME	FUNCTION	DFLT
0	LDSMIHLDER	Load SMI handler into SMM space: 1 = enable access to SMM space during non-SMI cycle, 0 = disable access to SMM space during normal cycle.	0
1	MOVRLYEN	Memory Overlay Enable: This function allows access to the standard memory space that is otherwise hidden beneath SMM space during SMM. When high, the standard memory space at addresses 20000-3FFFFH or 60000-7FFFFH(depending on bit 2 below) will be accessible at addresses 40000-5FFFFH during SMM. When low, addresses 40000-5FFFFH access standard memory space whether in SMM or not.	0
2	SMMMAPSEL	SMM Memory Map Select: When high, SMM physical memory at A0000-BFFFFH will be remapped to logical addresses 60000-7FFFFH. When low, SMM physical memory at A0000-BFFFFH will be remapped to logical addresses 20000-3FFFFH.	0
3	SMMDETECT	SMM Detect: When low, the SMIACT# input will be used to indicate that SMM is in progress. When high, the SMI# input will be used to indicate that SMM is in porgress. This is used for internal functions such as holding off solft resets during SMM.	0
4	Reserved		0
5	SMIFLUSHIN	SMI Flush In: When high, the CPU's internal cache will automatically be flushed upon entry to SMM, as detected by either SMIACT# or SMI# (see bit 3 above). When low, SMM will have no effect on the FLUSH# output pin.	0
6	SMIFLUSHOUT	SMI Flush Out: When high, the CPU's internal cache will automatically be flushed upon exit from SMM, as detected by either SMIACT# or SMI#(see bit 3 above). When low, SMM will have no effect on the FLUSH# output pin.	0
7	SMMKENDIS	SMM KEN disable: When high, KEN# will be held inactive(high) during SMM mode. When low, KEN# will function normally within SMM.	0
8	KDISSMMREG	SMM region KEN disable: When high, KEN# will be held inactive during access to SMM region, which is 20000H-3FFFFH or 60000H-7FFFFH depends on bit 2. When low, KEN# will function normally within the SMM region.	0

9	SMISEL	SMI Select: When high, the PMI output timing will be compatible with an SMI input, and the SMIRDY# and IIBEN# outputs willl be enabled to their nominal functions. When low, the PMI output timing will be compatible with the IRQX on the AT Bus, and the SMIRDY# output will be disabled	1
10	Reserved		0
11	SMMMSKA20	SMM Mask A20: When low, the A20M# signal will be set high during SMM, which unmasks A20. When high, the A20M# signal will be set low during SMM, which masks A20.	0
12	Reserved	.	0
13	SMMMAPD	SMM Memory Map using D segment: When high, SMM physical memory at B0000-BFFFFH will be remapped to logical addresses D0000-DFFFFH. When low, bit 2 above will be used for SMM memory remap instead.	0
14	SMMMAPE	SMM Memory Map using E segment: When high, SMM physical memory at A0000-AFFFFH will be remapped to logical addresses E0000-EFFFFH. When low, bit 2 above will be used for SMM memory remap instead.	0
15	SMISTRTSEL	SMI Start Select: When high, the standard ADS# input will be used to start SMM bus cycles. When low, the SMIADS# input will be used to start SMM bus cycles.	0

4.1.4 SYS Miscellaneous Control Register 2 — Configuration Index 104H

BIT	NAME	FUNCTION	DFLT
0	SMIHLDOFRST	Enable Hold-Off of SRESET during SMI cycles : 0 = Disabled; 1 = Enabled.	1
1	LCLKDIS	KEN disable always: When low, KEN# will be generated for all local memory cycles. When high, KEN# will be forced to inactive state for all cycles.	0
2	KFLUSH	Cache Flush: A high to low transition of this bit will generate a flush pulse to the CPU. Writing this bit high only has no effect.	0
3	Reserved		0
4	Reserved	.	0
5	Reserved		0
6	Reserved		1
9:7	Reserved		000
10	Reserved		0
11	Reserved		0
12	Reserved		1
13	ENRDYN#	Generate RDY# at the end of a burst cycle: 0 = RDY# will be generated, 1 = RDY# will not be generated.	1
14	LMABLOCK	Local Memory Access at A0000-BFFFFH Lock: This bit provides an option to lock register 103H bit 0 in a disabled state, thereby prohibiting any further access to SMM space from normal mode. This bit can only be written once.	0
15	SHDWRLOCK	Shadow RAM Write Lock: This bit provides an option to write lock all shadow RAM (C0000-FFFFFH) thereby prohibiting any further writes to shadow RAM memory. This effectively locks bits 12:0 of register 201H at a low level. This bit can be written only once.	0

4.1.5 Parity Address Register 1			Configuration Index 105H
BIT	NAME	FUNCTION	DFLT
1:0	Reserved		XX
15:2	PARADR<15:2>	Parity Error Address <15:2>	0000H

4.1.6 Parity Address Register 2			Configuration Index 106H
BIT	NAME	FUNCTION	DFLT
11:0	PARADR<27:16>	Parity Error Address <27:16>	000H
15:12	PARBE<3:0>	Byte Enables <3:0> for Parity Error Address	0H

4.1.7 Shadow Register for Programmable Range 0/1			Configuration Index 080H
BIT	BYTE ADD	REGISTER DESCRIPTION	DFLT
7:0	Index 020H/021H	Shadow register for programmable range 0 at index 020H/021H	00H
15:8	Index 022H/023H	Shadow register for programmable range 1 at index 022H/023H	00H

4.1.8 Shadow Register for Programmable Range 2/3			Configuration Index 081H
BIT	BYTE ADD	REGISTER DESCRIPTION	DFLT
7:0	Index 024H/025H	Shadow register for programmable range 2 at index 024H/025H	00H
15:8	Index 026H/027H	Shadow register for programmable range 3 at index 026H/027H	00H

4.1.9 RTC Shadow Register			Configuration Index 086H
BIT	BYTE ADD	REGISTER DESCRIPTION	DFLT
7:0	70H	RTC Index Register	00H
15:8	Reserved		XXH

4.1.10 Modular Clock Control Register		Configuration Index 118H	
BIT	NAME	FUNCTION	DFLT
0	CPUMODCLKEN	CPU Modular Clock Enable : 0 = CPU Modular Clock is disabled. 1 = CPU Modular Clock is enabled.	0
1	VLCLKSTPEN	VL Clock Stop Enable : If high, the VLCLK output (CPUCLKIO) will be stopped during STOP CLOCK state. If low, this clock will always be running.	1
4:2	Reserved		5H
7:5	Reserved		XX
8	MDCHGIMD	Mode Change Immediate: When high, PMC Mode changes will occur immediately upon request; when low, mode changes will only occur at the end of a CPU Bus cycle or when the CPU Bus is idle.	0
10:9	Reserved		XX
11	SLWATCKEN	SLOW AT Clock Enable : If low, HS1XCLK (and AT clock) will always be at high speed. If high, HS1XCLK (and AT clock) will be divided down together with the CPU clock.	0
12	Reserved		0
13	Reserved		0
14	Reserved		0
15	Reserved		0

4.1.11 Burst Bus Control Register		Configuration Index 180H	
BIT	NAME	FUNCTION	DFLT
2:0	Reserved		7H
3	R1GIDEEN	REDWOOD1 Global Turbo IDE Enable : When low, Turbo IDE is disabled. When high, Turbo IDE is enabled.	0
4	Reserved		0
5	Reserved		0
6	Reserved		X
9:7	Reserved		7H
12:10	Reserved		7H
14:13	Reserved		3H
15	SECIDEEN	Secondary IDE drive Enable : If high, secondary IDE addresses are used: 170H-177H for IDECS0# and 376H-377H for IDECS1#. If low, primary addresses are used : 1F0H-1F7H for IDECS0# and 3F6H-3F7H for IDECS1#.	0

4.2 REDWOOD 1 Pin Function Select Registers

4.2.0 REDWOOD 1 Pin Select Register 1		Configuration Index 110H	
BIT	NAME	FUNCTION	DFLT
0	Reserved		0
1	Reserved		0

2	TAGCSSEL	TAG Chip Select: This bit defines the function of LOCK#/CA13/TAGCS#/BUSYI pin. If index register 100H, bit 1 is high, this pin is BUSYI input. Furthermore, if index register 100H, bit 4 is low, this pin is LOCK# from the CPU. If index register 100H, bit 4 is high and this bit is low, the pin becomes TAG RAM Chip Select # output. If index register 100H, bit 4 is high and this bit is also high, the pin becomes CA13 (Cache Address 13 for level 2 cache).	0
3	LOCKPINSEL	LOCK# Pin Select: If index register 100H, bit 1 is low and this bit is also low, HITM#/LOCK# pin is the function of HITM#. If this bit is high, it is LOCK# function from the CPU.	0
4	CCSPINEN#	CCS PIN Enable # : This bit defines the functions of CCS<3:0>#. If low, those pins are Cache Chip Select <3:0>#. If high, these pins become FBE#, ACPWR, VLB and LB respectively. This bit will be overwritten by index register 100H, bit 0 being high.	0
5	TAGDEN#	TAG RAM Data bus ENable # : This bit defines the function of TAG Data <7:0>. If low, TAGD<7:0> are the normal TAG Data bits. If high, these pins become the optional HIT# and PC<9:4>. This bit will be overwritten by index register 100H, bit 0 being high.	0
6	Reserved		0
7	Reserved		0
8	GPIOC0PINEN#	GPIOC0 PIN ENable # : This bit defines the function of PC2 further. If index register 112H, bit 2 and 110H, bit 7 are high, and this bit is low, PC2 is redefined as GPIOC0. Use index register 016H, bits 10 and 8 to control the function of GPIOC0. If this bit is also high, then PC2 is GPCS1#.	0
9	Reserved		0
10	HTRGOUTEN	HTRGOUT ENable : If low, PC3 pin is the GPCS2# output. If high, PC3 is the HTRGOUT indicating an overheated condition. However, this bit will take effect only if index register 112H, bit 3 is high.	0
11	GPIOA0PINEN#	GPIOA0 PIN ENable # : This bit defines the function of PC7 pin. If index register 112H, bit 7 is high and this bit is low, PC7 becomes GPIOA0 and will be controller by index register 014H, bits 0 and 2. If 112H, bit 7 and this bit are both high, PC7 becomes EXTACT2 input.	0
12	GPIOA1PINEN#	GPIOA1 PIN ENable # : This bit defines the function of PC8 pin. If index register 112H, bit 8 is high and this bit is low, PC8 becomes GPIOA1 and will be controller by index register 014H, bits 1 and 3.	0
15:13	Reserved		000

4.2.1 REDWOOD 1 Pin Select Register 2		Configuration Index 111H	
BIT	NAME	FUNCTION	DFLT
0	OPGPEXTEN	Optional GPEXT Enable : If index register 111H, bit 12 is high and this bit is low, then pin GPIO0/FRCSLW/GPEXT is the FRCSLW input. If this bit is also high, then the pin function is GPEXT output.	0
1	Reserved		0
2	EXTACT3PINEN	EXTACT3 Pin Enable : If index register 112H, bit 4 below is high and this bit is low, PC4 pin is General Purpose Chip Select (GPCS3#). If this bit is also high, then it is EXTACT3 input.	0

3	NMIPINEN	NMI Pin Enable : If index register 100H, bit 0 and 111H, bit 6 are both high and this bit is low, DRTWE#/WAKE1/GPIOB1 pin becomes NMI input for parity error address latching.	0
4	DIRTYPINEN#	DIRTY PIN ENable #: This bit defines the function of DIRTY/WAKE0/GPIOB0 pin. If this bit is low, the pin is the DIRTY signal. If high, the function will be determined by bit 5 of the same index register (see below).	0
5	GPIOB0PINEN	GPIOB0 PIN ENable : This bit defines the function of DIRTY/WAKE0/GPIOB0 pin. If bit 4 above is high and this bit is low, the pin is the WAKE0 input. If bit 4 above is high and this bit is also high , the pin becomes GPIOB0. Use index register 14H, bits 6 and 4 to control the GPIOB1 function.	0
6	DRTWEPINEN#	DRTWE# PIN ENable #: This bit defines the function of DRTWE#/WAKE1/GPIOB1 pin. If this bit is low, the pin is the DRTWE# (Dirty Write Enable #) signal. If high, the function will be determined by bits 3 and 7 of the same index register.	0
7	GPIOB1PINEN	GPIOB1 PIN ENable : This bit defines the function of DRTWE#/WAKE1/GPIOB1 pin. If bits 3 and 6 above are high and this bit is low, the pin is the WAKE1 input. If all bits are high , the pin becomes GPIOB1. Use index register 14H, bits 7 and 5 to control the GPIOB1 function.	0
8	KBRSTPINEN	KB reset Pin Enable : This bit defines the function of KBRST pin. If this bit is low , then the pin is the KBRST (keyboard controller reset) input. If this bit is high , then the function will be determined by bits 9 to 11 below.	0
9	Reserved		0
10	Reserved		0
11	GPIOC1PINEN	GPIOC1 PIN ENable : This bit defines the function of KBRST pin further. If bits 8, 9, 10 are all high and this bit is low, the pin becomes GPIOC1. Use index register 16H, bits 11 and 9 to control the GPIOC1 function. If bits 8, 9, 10 and 11 are all high, then the pin is GPCS0# output.	0
12	GPIO0PINEN#	GPIO0 PIN ENable # : This bit defines the function of GPIO0/FRCSLW/GPEXT pin. If low, the pin is GPIO0. If high, use index 111H bit 0 to select the function.	0
13	GPIO1PINEN#	GPIO1 PIN ENable # : This bit defines the function of GPIO1 pin. If low, the pin is GPIO1. If high, use index register 112H, bit 13 below to determine its function.	0
14	GPIO2PINEN#	GPIO2 PIN ENable # : This bit defines the function of GPIO2/RING pin. If low, the pin is GPIO2. If high, the pin becomes RING input if index register 100H, bit 0 is low. Or it is MDEN# output if index register 100H, bit 0 is high.	0
15	GPIO3PINEN#	GPIO3 PIN ENable # : This bit defines the function of GPIO3 pin. If low, the pin is GPIO3. If high, use index register 112H, bit 15 below to determine its function.	0

4.2.2 REDWOOD 1 Pin Select Register 3		Configuration Index 112H	
BIT	NAME	FUNCTION	DFLT
0	PC0PINEN#	PC0 PIN ENable # : This bit defines the function of PC0. If low, this pin is the PC0 function. If high, this output becomes the TSTOUT (test output).	0

1	Reserved		0
2	PC2PINEN#	PC2 PIN ENable # : This bit defines the function of PC2. If low, this pin is the PC2 function. If high, the function of ths pin will depends upon index register 110H, bits 8 and 9.	0
3	PC3PINEN#	PC3 PIN ENable # : This bit defines the function of PC3. If low, this pin is the PC3 function. If high, the function of ths pin will depends upon index register 110H, bit 10.	0
4	PC4PINEN#	PC4 PIN ENable # : This bit defines the function of PC4. If low, this pin is the PC4 function. If high, it becomes GPCS3# output.	0
5	PC5PINEN#	PC5 PIN ENable # : This bit defines the function of PC5. If low, this pin is the PC5 function. If high, it becomes SPLEDFLSH (Suspend LED Flasher) output.	0
6	PC6PINEN#	PC6 PIN ENable # : This bit defines the function of PC6. If low, this pin is the PC6 function. If high, it becomes LBLEDFLSH (Low Battery LED Flasher) output.	0
7	PC7PINEN#	PC7 PIN ENable # : This bit defines the function of PC7. If low, this pin is the PC7 function. If high, the function of ths pin will depends upon index register 110H, bit 11.	0
8	PC8PINEN#	PC8 PIN ENable # : This bit defines the function of PC8. If low, this pin is the PC8 function. If high, the function of ths pin will depends upon index register 110H, bit 12.	0
9	PC9PINEN#	PC9 PIN ENable # : This bit defines the function of PC9. If low, this pin is the PC9 function. If high, the function of this pin is GPEXT.	0
10	Reserved		0
11	Reserved		0
12	EXTACT0PINEN	EXTACT0 Pin Enable : If this bit is high, then NMI/EXTACT0 pin is EXTACT0. If low, then it is NMI input. However, this bit is only valid if index register 100H, bit 0 is low.	0
13	KBCLKOPINEN	KB Clock Output Pin Enable : If index register 111H, bit 13 is high and this bit is low, GPIO1 becomes the input as KB GateA20 function. If this bit is also high, it is KB Clock Output.	0
14	387PINEN	387 Pin Enable : If high, a 387 coprocessor is installed in the system. Then CPURST/NPURST output will become NPURST function and FLUSH# will become IRQ13 output. This bit is valid only if index register 100H, bit 1 is high (386DX mode).	0
15	EXTACT1PINEN	EXTACT1 Pin Enable : If index register 111H, bit 15 is high and this bit also high, then GPIO3/EXTACT1 is EXTACT1 input.	0

4.3 DRAM Controller Register Specification

4.3.0 Shadow RAM Read Enable Control Register		Configuration Index 200H	
BIT	NAME	FUNCTION	DFLT
0	LMEMRDEN0	Local memory C0000H-C3FFFH read enable: 0 = Disabled; 1 = Enabled.	0
1	LMEMRDEN1	Local memory C4000H-C7FFFH read enable: 0 = Disabled; 1 = Enabled.	0
2	LMEMRDEN2	Local memory C8000H-CBFFFH read enable: 0 = Disabled; 1 = Enabled.	0
3	LMEMRDEN3	Local memory CC000H-CFFFFH read enable: 0 = Disabled; 1 = Enabled.	0

4	LMEMRDEN4	Local memory D0000H-D3FFFH read enable: 0 = Disabled; 1 = Enabled.	0
5	LMEMRDEN5	Local memory D4000H-D7FFFH read enable: 0 = Disabled; 1 = Enabled.	0
6	LMEMRDEN6	Local memory D8000H-DBFFFH read enable: 0 = Disabled; 1 = Enabled.	0
7	LMEMRDEN7	Local memory DC000H-DFFFFH read enable: 0 = Disabled; 1 = Enabled.	0
8	LMEMRDEN8	Local memory E0000H-E3FFFH read enable: 0 = Disabled; 1 = Enabled.	0
9	LMEMRDEN9	Local memory E4000H-E7FFFH read enable: 0 = Disabled; 1 = Enabled.	0
10	LMEMRDEN10	Local memory E8000H-EBFFFH read enable: 0 = Disabled; 1 = Enabled.	0
11	LMEMRDEN11	Local memory EC000H-EFFFFH read enable: 0 = Disabled; 1 = Enabled.	0
12	LMEMRDEN12	Local memory F0000H-FFFFFH read enable: 0 = Disabled; 1 = Enabled.	0
15:13	Reserved		0H

4.3.1 Shadow RAM Write Enable Control Register		Configuration Index 201H	
BIT	NAME	FUNCTION	DFLT
0	LMEMWREN0	Local memory C0000H-C3FFFH write enable: 0 = Disabled; 1 = Enabled.	0
1	LMEMWREN1	Local memory C4000H-C7FFFH write enable: 0 = Disabled; 1 = Enabled.	0
2	LMEMWREN2	Local memory C8000H-CBFFFH write enable: 0 = Disabled; 1 = Enabled.	0
3	LMEMWREN3	Local memory CC000H-CFFFFH write enable: 0 = Disabled; 1 = Enabled.	0
4	LMEMWREN4	Local memory D0000H-D3FFFH write enable: 0 = Disabled; 1 = Enabled.	0
5	LMEMWREN5	Local memory D4000H-D7FFFH write enable: 0 = Disabled; 1 = Enabled.	0
6	LMEMWREN6	Local memory D8000H-DBFFFH write enable: 0 = Disabled; 1 = Enabled.	0
7	LMEMWREN7	Local memory DC000H-DFFFFH write enable: 0 = Disabled; 1 = Enabled.	0
8	LMEMWREN8	Local memory E0000H-E3FFFH write enable: 0 = Disabled; 1 = Enabled.	0
9	LMEMWREN9	Local memory E4000H-E7FFFH write enable: 0 = Disabled; 1 = Enabled.	0
10	LMEMWREN10	Local memory E8000H-EBFFFH write enable: 0 = Disabled; 1 = Enabled.	0
11	LMEMWREN11	Local memory EC000H-EFFFFH write enable: 0 = Disabled; 1 = Enabled.	0
12	LMEMWREN12	Local memory F0000H-FFFFFH write enable: 0 = Disabled; 1 = Enabled.	0
15:13	Reserved		0H

4.3.2 Bank 0 Control Register		Configuration Index 202H	
BIT	NAME	FUNCTION	DFLT
7:0	B0A<27:20>	Bank 0 starting address <27:20>	00H
10:8	B0S<2:0>	Bank 0 DRAM size Bits <2:0> DRAM size Bits <2:0> DRAM size 000 256K 100 4M 001 512K 101 Reserved 010 1M 110 16M 011 2M 111 Reserved	000
11	BANKEN0	Bank 0 enable : 0 = Disabled, 1 = Enabled	1
12	ENMDEN0N	Enable MDEN# for Bank 0 : 0 = Enabled, 1 = Disabled	0
15:13	COLADR0<2:0>	Number of column address bits for Bank 0 <2:0> Bits <2:0> Number of column address bits 000 8 bits 001 9 bits 010 10 bits 011 11 bits 100 12 bits 11X Reserved 1X1 Reserved	000

4.3.3 Bank 1 Control Register		Configuration Index 203H	
BIT	NAME	FUNCTION	DFLT
7:0	B1A<27:20>	Bank 1 starting address <27:20>	00H
10:8	B1S<2:0>	Bank 1 DRAM size Bits <2:0> DRAM size Bits <2:0> DRAM size 000 256K 100 4M 001 512K 101 Reserved 010 1M 110 16M 011 2M 111 Reserved	000
11	BANKEN1	Bank 1 enable : 0 = Disabled, 1 = Enabled	0
12	ENMDEN1N	Enable MDEN# for Bank 1 : 0 = Enabled, 1 = Disabled	0
15:13	COLADR1<2:0>	Number of column address bits for Bank 1 <2:0> Bits <2:0> Number of column address bits 000 8 bits 001 9 bits 010 10 bits 011 11 bits 100 12 bits 11X Reserved 1X1 Reserved	000

4.3.4 Bank 0/1 Timing Control Register		Configuration Index 204H	
BIT	NAME	FUNCTION	DFLT
1:0	B01WRCPW<1:0>	Bank 0 and Bank 1 write CAS cycle time <1:0> Bits <1:0> — Write CAS pulse cycle time 0 0 — Reserved 0 1 — 1T 1 0 — 2T 1 1 — 3T	11
2	MA01WRDLY	Bank 0 and Bank 1 write MA delay : 0 = delay by 0.5T, 1 = no delay	1
4:3	B01RDCPW<1:0>	Bank 0 and Bank 1 read CAS cycle time <1:0> Bits <1:0> — Read CAS pulse cycle time 0 0 — 1T 0 1 — 2T 1 0 — 3T 1 1 — 4T	11
5	MA01RDDLY	Bank 0 and Bank 1 read MA delay : 0 = no delay, 1 = delay by 0.5 T state	1
6	B01CPRE	Bank 0 and Bank 1 CAS precharge : 0 = 0.5 T, 1 = 1.0 T	1
7	B01RTMA	Bank 0 and Bank 1 RAS To MA delay : 0 = 0.5 T, 1 = 1.0 T	1
8	B01MATC	Bank 0 and Bank 1 MA To CAS delay : 0 = 0.5 T, 1 = 1.0 T	1
11:9	B01RPRE<2:0>	Bank 0 and Bank 1 RAS PREcharge time <2:0> Bits <2:0> — Precharge time — Bits <2:0> — Precharge time 0 0 0 — Reserved — 1 0 0 — 2.5 T 0 0 1 — Reserved — 1 0 1 — 3.0 T 0 1 0 — 1.5 T — 1 1 0 — 3.5 T 0 1 1 — 2.0 T — 1 1 1 — 4.0 T	111
12	Reserved		1
13	BNK01_ITL	Bank 0 and Bank 1 Interleave Enable : 0 = Interleave Disabled, 1 = Interleave Enabled	0
15:14	Reserved		XH

4.3.5 Bank 2 Control Register		Configuration Index 205H	
BIT	NAME	FUNCTION	DFLT
7:0	B2<27:20>	Bank 2 starting address <27:20>	00H
10:8	B2<2:0>	Bank 2 DRAM size Bits <2:0> — DRAM size — Bits <2:0> — DRAM size 0 0 0 — 256K — 1 0 0 — 4M 0 0 1 — 512K — 1 0 1 — Reserved 0 1 0 — 1M — 1 1 0 — 16M 0 1 1 — 2M — 1 1 1 — Reserved	000
11	BANKEN2	Bank 2 enable : 0 = Disabled, 1 = Enabled	0
12	ENMDEN2N	Enable MDEN# for Bank 2 : 0 = Enabled, 1 = Disabled	0

15:13	COLADR2<2:0>	Number of column address bits for Bank 2 <2:0> Bits <2:0> Number of column address bits 0 0 0 8 bits 0 0 1 9 bits 0 1 0 10 bits 0 1 1 11 bits 1 0 0 12 bits 1 1 X Reserved 1 X 1 Reserved	000

4.3.6 Bank 3 Control Register		Configuration Index 206H	
BIT	NAME	FUNCTION	DFLT
7:0	B3A<27:20>	Bank 3 starting address <27:20>	00H
10:8	B3S<2:0>	Bank 3 DRAM size Bits <2:0> DRAM size Bits <2:0> DRAM size 0 0 0 256K 1 0 0 4M 0 0 1 512K 1 0 1 Reserved 0 1 0 1M 1 1 0 16M 0 1 1 2M 1 1 1 Reserved	000
11	BANKEN3	Bank 3 enable : 0 = Disabled, 1 = Enabled	0
12	ENMDEN3N	Enable MDEN# for Bank 3 : 0 = Enabled, 1 = Disabled	0
15:13	COLADR3<2:0>	Number of column address bits for Bank 3 <2:0> Bits <2:0> Number of column address bits 0 0 0 8 bits 0 0 1 9 bits 0 1 0 10 bits 0 1 1 11 bits 1 0 0 12 bits 1 1 X Reserved 1 X 1 Reserved	000

4.3.7 Bank 2/3 Timing Control Register		Configuration Index 207H	
BIT	NAME	FUNCTION	DFLT
1:0	B23WRCPW<1:0>	Bank 2 and Bank 3 write CAS cycle time <1:0> Bits <1:0> Write CAS pulse cycle time 0 0 Reserved 0 1 1T 1 0 2T 1 1 3T	11
2	MA23WRDLY	Bank 2 and Bank 3 write MA delay : 0 = delay by 0.5T, 1 = no delay	1
4:3	B23RDCPW<1:0>	Bank 2 and Bank 3 read CAS cycle time <1:0> Bits <1:0> Read CAS pulse cycle time 0 0 1T 0 1 2T 1 0 3T 1 1 4T	11

5	MA23RDDLY	Bank 2 and Bank 3 read MA delay : 0 = no delay, 1 = delay by 0.5 T state	1
6	B23CPRE	Bank 2 and Bank 3 CAS precharge : 0 = 0.5 T, 1 = 1.0 T	1
7	B23RTMA	Bank 2 and Bank 3 RAS To MA delay : 0 = 0.5 T, 1 = 1.0 T	1
8	B23MATC	Bank 2 and Bank 3 MA To CAS delay : 0 = 0.5 T, 1 = 1.0 T	1
11:9	B23RPRE<2:0>	Bank 2 and Bank 3 RAS PREcharge time <2:0> Bits <2:0> Precharge time Bits <2:0> Precharge time 0 0 0 Reserved 1 0 0 2.5 T 0 0 1 Reserved 1 0 1 3.0 T 0 1 0 1.5 T 1 1 0 3.5 T 0 1 1 2.0 T 1 1 1 4.0 T	111
12	Reserved		1
13	BNK23_ITL	Bank 2 and Bank 3 Interleave Enable : 0 = Interleave Disabled, 1 = Interleave Enabled	0
15:14	Reserved		XH

4.3.8 Bank 4 Control Register — Configuration Index 208H

BIT	NAME	FUNCTION	DFLT
7:0	B4A<27:20>	Bank 4 starting address <27:20>	00H
10:8	B4S<2:0>	Bank 4 DRAM size Bits <2:0> DRAM size Bits <2:0> DRAM size 0 0 0 256K 1 0 0 4M 0 0 1 512K 1 0 1 Reserved 0 1 0 1M 1 1 0 16M 0 1 1 2M 1 1 1 Reserved	000
11	BANKEN4	Bank 4 enable : 0 = Disabled, 1 = Enabled	0
12	ENMDEN4N	Enable MDEN# for Bank 4 : 0 = Enabled, 1 = Disabled	0
15:13	COLADR4<2:0>	Number of column address bits for Bank 4 <2:0> Bits <2:0> Number of column address bits 0 0 0 8 bits 0 0 1 9 bits 0 1 0 10 bits 0 1 1 11 bits 1 0 0 12 bits 1 1 X Reserved 1 X 1 Reserved	000

4.3.9 Bank 5 Control Register — Configuration Index 209H

BIT	NAME	FUNCTION	DFLT
7:0	B5A<27:20>	Bank 5 starting address <27:20>	00H
10:8	B5S<2:0>	Bank 5 DRAM size Bits <2:0> DRAM size Bits <2:0> DRAM size 0 0 0 256K 1 0 0 4M 0 0 1 512K 1 0 1 Reserved 0 1 0 1M 1 1 0 16M 0 1 1 2M 1 1 1 Reserved	000
11	BANKEN5	Bank 5 enable : 0 = Disabled, 1 = Enabled	0

12	ENMDEN5N	Enable MDEN# for Bank 5 : 0 = Enabled, 1 = Disabled	0
15:13	COLADR5<2:0>	Number of column address bits for Bank 5 <2:0> Bits <2:0> — Number of column address bits 0 0 0 — 8 bits 0 0 1 — 9 bits 0 1 0 — 10 bits 0 1 1 — 11 bits 1 0 0 — 12 bits 1 1 X — Reserved 1 X 1 — Reserved	000

4.3.10 Bank 4/5 Timing Control Register		Configuration Index 20AH	
BIT	NAME	FUNCTION	DFLT
1:0	B45WRCPW<1:0>	Bank 4 and Bank 5 write CAS cycle time <1:0> Bits <1:0> — Write CAS pulse cycle time 0 0 — Reserved 0 1 — 1T 1 0 — 2T 1 1 — 3T	11
2	MA45WRDLY	Bank 4 and Bank 5 write MA delay : 0 = delay by 0.5T, 1 = no delay	1
4:3	B45RDCPW<1:0>	Bank 4 and Bank 5 read CAS cycle time <1:0> Bits <1:0> — Read CAS pulse cycle time 0 0 — 1T 0 1 — 2T 1 0 — 3T 1 1 — 4T	11
5	MA45RDDLY	Bank 4 and Bank 5 read MA delay : 0 = no delay, 1 = delay by 0.5 T state	1
6	B45CPRE	Bank 4 and Bank 5 CAS precharge : 0 = 0.5 T, 1 = 1.0 T	1
7	B45RTMA	Bank 4 and Bank 5 RAS To MA delay : 0 = 0.5 T, 1 = 1.0 T	1
8	B45MATC	Bank 4 and Bank 5 MA To CAS delay : 0 = 0.5 T, 1 = 1.0 T	1
11:9	B45RPRE<2:0>	Bank 4 and Bank 5 RAS PREcharge time <2:0> Bits <2:0> — Precharge time 0 0 0 — Reserved 0 0 1 — Reserved 0 1 0 — 1.5 T 0 1 1 — 2.0 T 1 0 0 — 2.5 T 1 0 1 — 3.0 T 1 1 0 — 3.5 T 1 1 1 — 4.0 T	111
12	Reserved		1
13	BNK45_ITL	Bank 4 and Bank 5 Interleave Enable : 0 = Interleave Disabled, 1 = Interleave Enabled	0
15:14	Reserved		XH

4.3.11 DRAM Configuration Register 1		Configuration Index 20BH	
BIT	NAME	FUNCTION	DFLT
0	SIXRASEN	Six RAS# Control Line Enable : If high, CAS0B# = RAS1#, CAS1B# = RAS3#, CAS2B# = RAS5# and CAS3B# is not used. This feature is to support six independent DRAM banks instead of 3 pairs. RAS1# becomes RAS2# and RAS2# becomes RAS4#.	0
1	Reserved		X
2	Reserved		X
3	BRSTWREN	Burst Write Enable 0 = Disabled, 1 = Enabled.	0
6:4	PS<2:0>	DRAM page size <2:0> Bits <2:0> Page Size 0 0 0 1K 0 0 1 2K 0 1 0 4K 0 1 1 8K 1 0 0 16K 1 0 1 32K 1 1 X Reserved	000
7	Reserved		0
8	Reserved		X
9	RONLYRF	DRAM refresh scheme : 0 = CAS before RAS refresh, 1 = RAS only refresh	0
11:10	RFRPRE<1:0>	RAS precharge time for refresh cycles <1:0> Bits<1:0> RAS precharge time 0 0 5 T 0 1 4 T 1 0 3 T 1 1 2 T	00
13:12	RFRPW<1:0>	RAS pulse width for refresh cycles <1:0> Bits<1:0> RAS pulse width 0 0 5 T 0 1 4 T 1 0 3 T 1 1 2 T	00
14	XWITDOFFR	Extra wait state for lead-off read cycles : 0 = no additional wait state, 1 = add one extra wait state	1
15	XWITDOFFW	Extra wait state for lead-off write cycles : 0 = no additional wait state, 1 = add one extra wait state	1

4.3.12 DRAM Configuration Register 2		Configuration Index 20CH	
BIT	NAME	FUNCTION	DFLT
0	Reserved		0
1	Reserved		0
8:2	Reserved		XXH
9	ENPARADRL	Enable Parity Error Address Latch : 0 = Disabled; 1 = Enabled.	0
10	ENPARCK0	Enable parity check for Bank 0 : 0 = Disabled, 1 = Enabled	0
11	ENPARCK1	Enable parity check for Bank 1 : 0 = Disabled, 1 = Enabled	0
12	ENPARCK2	Enable parity check for Bank 2 : 0 = Disabled, 1 = Enabled	0
13	ENPARCK3	Enable parity check for Bank 3 : 0 = Disabled, 1 = Enabled	0
14	ENPARCK4	Enable parity check for Bank 4 : 0 = Disabled, 1 = Enabled	0

15	ENPARCK5	Enable parity check for Bank 5 : 0 = Disabled, 1 = Enabled	0

4.3.13 Reserved			Configuration Index 20DH
BIT	NAME	FUNCTION	DFLT
3:0	Reserved		0111
7:4	Reserved		0111
11:8	Reserved		0111
15:12	Reserved		0111

4.3.14 Reserved			Configuration Index 20EH
BIT	NAME	FUNCTION	DFLT
3:0	Reserved		0111
7:4	Reserved		0111
11:8	Reserved		0111
15:12	Reserved		XXXX

4.3.15 DRAM Configuration Register 5			Configuration Index 20FH
BIT	NAME	FUNCTION	DFLT
0	Reserved		0
1	FLASHENB	Flash Enable: When high, ROMCS# will be generated for memory writes as well as memory reads. When low, ROMCS# will only be generated for memory reads.	0
7:2	Reserved		XXH
9:8	Reserved		XX
10	ENC0ROMCS	Enable ROMCS# for C0000H-C7FFFH region. 0 = ROMCS# will not be active for this region. 1 = ROMCS# will be active.	0
11	ENC8ROMCS	Enable ROMCS# for C8000H-CFFFFH region. 0 = ROMCS# will not be active for this region. 1 = ROMCS# will be active.	0
12	END0ROMCS	Enable ROMCS# for D0000H-D7FFFH region. 0 = ROMCS# will not be active for this region. 1 = ROMCS# will be active.	0
13	END8ROMCS	Enable ROMCS# for D8000H-DFFFFH region. 0 = ROMCS# will not be active for this region. 1 = ROMCS# will be active.	0
14	ENE0ROMCS	Enable ROMCS# for E0000H-E7FFFH region. 0 = ROMCS# will not be active for this region. 1 = ROMCS# will be active.	0
15	ENE8ROMCS	Enable ROMCS# for E8000H-EFFFFH region. 0 = ROMCS# will not be active for this region. 1 = ROMCS# will be active.	0

4.4 Power Management Controller Register Specification

4.4.0 PMC Clock Control Register			Configuration Index 000H
BIT	NAME	FUNCTION	DFLT
2:0	CNCLKSEL<2:0>	Conserve CLK Selects: Bits<2:0> Divide By Bits<2:0> Divide By 0H 1 4H 16 1H 2 5H 32 2H 4 6H 64 3H 8 7H Reserved	0H
3	CNSRVEN	Conserve Mode Enable: When high Conserve Mode is enabled, when low it is not.	0
6:4	SLCLKSEL<2:0>	Slow CLK Selects: Bits<2:0> Divide By Bits<2:0> Divide By 0H 1 4H 16 1H 2 5H 32 2H 4 6H 64 3H 8 7H STOPPED	0H
7	SLWCLKEN	Slow Clock Enable: When high, the slow clock function is enabled and will be active during Doze, Sleep or Suspend Mode if DZSLWEN, SLPSLWEN or SPNDSLWEN is enabled respectively (register 000H bits 10, 9 ,8) When low, the slow clock option will never be selected.	0
8	SLPSLWEN	Sleep Mode, Slow Clock Enable: When high, Sleep Mode will be switched to the Low Clock Frequency, as set by index register 000H bits 6:4. Note that SLWCLKEN (register 000H bit 7) must be set to enable this feature.	0
9	DZSLWEN	Doze Mode, Slow Clock Enable: When high, Doze Mode will be switched to the Low Clock Frequency, as set by index register 000H bits 6:4. Note that SLWCLKEN (register 000H bit 7) must be set to enable this feature.	0
10	SPNDSLWEN	Suspend Mode, Slow Clock Enable: When high, Suspend Mode will be switched to the Low Clock Frequency, as set by index register 000H, bits 6:4. Note that SLWCLKEN (register 000H bit 7) must be set to enable this feature.	0
11	LBSLWEN	Low Battery Slow Enable: When high the CPUCLK will be switched to slow speed as set in register 000H, bits 6:4 whenever the LB or VLB input is high; when low, there will be no change in CPUCLK directly related to the LB input.	0
12	Reserved		0
13	Reserved		0
14	LBST	Low Battery Status: This bit reflects the current status of the LB input. This bit is read only.	X
15	VLBST	Very Low Battery Status: This bit reflects the current status of the VLB input. This bit is read only.	X

4.4.1 Power Management Status Register		Configuration Index 001H	
BIT	NAME	FUNCTION	DFLT
2:0	WAKESRC<2:0>	Wake-up Source: Bits<2:0> Source 0H None 1H RING 2H RTC Interrupt 3H SWTCH 4H GP Timer Compare 5H WAKE0 6H WAKE1 7H Clear Wake Source These bits are read only. They must be cleared after reading by a write of 7H.	0H
3	ACPWR	AC Power: This bit indicates the current status of the ACPWR input pin. This bit is read only.	X
8:4	PMISRC<4:0>	Power Management Interrupt: Bits<4:0> Source 00H None 01H IRQ input 02H LB Change 03H Suspend Timeout 04H Sleep Timeout 05H Doze Timeout 06H Generic Timeout 07H Generic Activity 08H Primary Activity 09H Secondary Activity 0AH Reserved 0BH SWTCH 0CH ACPWR 0DH Programmable Timers Timeout 0EH GP Timer Compare 0FH Reserved 10H Reserved 11H RTC 12H Rescheduled PMI 13H Software SMI All others Reserved These bits are read only. They must be cleared after reading by a write of 1FH.	0H
9	RESUME	Resume: When high this bit indicates that a SUSPEND has taken place such that the previous system state must be restored. This bit should be written low upon resuming.	0
10	WAKE0STATUS	Wake 0 Status : This bit reflects the status of WAKE0 input pin.	0
11	WAKE1STATUS	Wake 1 Status : This bit reflects the status of WAKE1 input pin.	0
12	Reserved		0

15:13	PMMD<2:0>	Power Management Mode: Bits<2:0> — State 0H — STANDBY 1H — ON 2H — CONSERVE 3H — DOZE 4H — SLEEP 5H — SUSPEND 7:6H — Reserved These bits are read/write. A write of 6H or 7H has no effect on the Power Management Mode.	0H

4.4.2 Activity Source Register — Configuration Index 002H

BIT	NAME	FUNCTION	DFLT
0	VIDACTV	Video Active: When Video access is detected this bit will be set high. Writing "0" to this bit will clear it; writing "1" will have no effect.	0
1	HDACTV	Hard Disk Active: When Hard Disk access is detected this bit will be set high. This bit is read only, but will be cleared on any write to this register. Writing "0" to this bit will clear it; writing "1" will have no effect.	0
2	FLPACTV	Floppy Disk Active: When Floppy Disk access is detected this bit will be set high. This bit is read only, but will be cleared on any write to this register. Writing "0" to this bit will clear it; writing "1" will have no effect.	0
3	KBDACTV	Keyboard Active: When Keyboard access is detected this bit will be set high. This bit is read only, but will be cleared on any write to this register. Writing "0" to this bit will clear it; writing "1" will have no effect.	0
4	SIOACTV	Serial I/O Active: When Serial I/O access is detected this bit will be set high. This bit is read only, but will be cleared on any write to this register. Writing "0" to this bit will clear it; writing "1" will have no effect.	0
5	PIOACTV	Parallel I/O Active: When Parallel I/O access is detected this bit will be set high. This bit is read only, but will be cleared on any write to this register. Writing "0" to this bit will clear it; writing "1" will have no effect.	0
6	PROG0ACTV	Programmable Range Monitor 0 Active: When Programmable Range 0 access is detected this bit will be set high. Writing "0" to this bit will clear it; writing "1" will have no effect.	0
7	PROG1ACTV	Programmable Range Monitor 1 Active: When Programmable Range 1 access is detected this bit will be set high. Writing "0" to this bit will clear it; writing "1" will have no effect.	0
8	PROG2ACTV	Programmable Range Monitor 2 Active: When Programmable Range 2 access is detected this bit will be set high. Writing "0" to this bit will clear it; writing "1" will have no effect.	0
9	PROG3ACTV	Programmable Range Monitor 3 Active: When Programmable Range 3 access is detected this bit will be set high. Writing "0" to this bit will clear it; writing "1" will have no effect.	0
10	Reserved		0
11	Reserved		0

12	EXT0ACTV	EXTACT 0 Active: When the EXTACT0 input is detected high this bit will be set high. Writing "0" to this bit will clear it; writing "1" will have no effect.	0
13	EXT1ACTV	EXTACT 1 Active: When the EXTACT1 input is detected high this bit will be set high. Writing "0" to this bit will clear it; writing "1" will have no effect.	0
14	EXT2ACTV	EXTACT 2 Active: When the EXTACT2 input is detected high this bit will be set high. Writing "0" to this bit will clear it; writing "1" will have no effect.	0
15	EXT3ACTV	EXTACT 3 Active: When the EXTACT3 input is detected high this bit will be set high. Writing "0" to this bit will clear it; writing "1" will have no effect.	0

4.4.3 Primary Activity Mask Register — Configuration Index 003H

BIT	NAME	FUNCTION	DFLT
0	PAMSKVID	Primary Activity Mask Video Accesses: When high Video accesses will not trigger the Primary Idle Detector.	1
1	PAMSKHD	Primary Activity Mask Hard Disk Accesses: When high Hard Disk accesses will not trigger the Primary Idle Detector.	1
2	PAMSKFLP	Primary Activity Mask Floppy Accesses: When high Floppy accesses will not trigger the Primary Idle Detector.	1
3	PAMSKKBD	Primary Activity Mask Keyboard Accesses: When high Keyboard access will not trigger the Primary Idle Detector.	1
4	PAMSKSIO	Primary Activity Mask Serial I/O Accesses: When high Serial I/O accesses will not trigger the Primary Idle Detector.	1
5	PAMSKPIO	Primary Activity Mask Parallel I/O Accesses: When high Parallel I/O accesses will not trigger the Primary Idle Detector.	1
6	PAMSKPROG0	Primary Activity Mask Programmable Range 0 : When high, any access to the programmable range 0 will not trigger the Primary Idle Detector.	1
7	PAMSKPROG1	Primary Activity Mask Programmable Range 1 : When high, any access to the programmable range 1 will not trigger the Primary Idle Detector.	1
8	PAMSKPROG2	Primary Activity Mask Programmable Range 2 : When high, any access to the programmable range 2 will not trigger the Primary Idle Detector.	1
9	PAMSKPROG3	Primary Activity Mask Programmable Range 3 : When high, any access to the programmable range 3 will not trigger the Primary Idle Detector.	1
10	Reserved		X
11	Reserved		X
12	PAMSKEACT0	Primary Activity Mask EXTACT0 : When high, EXTACT0 will not trigger the Primary Idle Detector.	1
13	PAMSKEACT1	Primary Activity Mask EXTACT1 : When high, EXTACT1 will not trigger the Primary Idle Detector.	1
14	PAMSKEACT2	Primary Activity Mask EXTACT2 : When high, EXTACT2 will not trigger the Primary Idle Detector.	1
15	PAMSKEACT3	Primary Activity Mask EXTACT3 : When high, EXTACT3 will not trigger the Primary Idle Detector.	1

4.4.4 PMI Mask Register			Configuration Index 004H
BIT	NAME	FUNCTION	DFLT
0	IMSKVID	PMI Mask Video Accesses: When high Video accesses will not trigger PMI.	1
1	IMSKHD	PMI Mask Hard Disk Accesses: When high Hard Disk accesses will not trigger PMI.	1
2	IMSKFLP	PMI Mask Floppy Accesses: When high Floppy accesses will not trigger PMI.	1
3	IMSKKBD	PMI Mask Keyboard Accesses: When high Keyboard access will not trigger PMI.	1
4	IMSKSIO	PMI Mask Serial I/O Accesses: When high Serial I/O accesses will not trigger PMI.	1
5	IMSKPIO	PMI Mask Parallel I/O Accesses: When high Parallel I/O accesses will not trigger PMI.	1
6	IMSKPROG0	PMI Mask Programmable Range 0 : When high, any access to the programmable range 0 will not trigger PMI.	1
7	IMSKPROG1	PMI Mask Programmable Range 1 : When high, any access to the programmable range 1 will not trigger PMI.	1
8	IMSKPROG2	PMI Mask Programmable Range 2 : When high, any access to the programmable range 2 will not trigger PMI.	1
9	IMSKPROG3	PMI Mask Programmable Range 3 : When high, any access to the programmable range 3 will not trigger PMI.	1
10	Reserved		X
11	Reserved		X
12	IMSKEACT0	PMI Mask EXTACT0 : When high, EXTACT0 will not trigger PMI.	1
13	IMSKEACT1	PMI Mask EXTACT1 : When high, EXTACT1 will not trigger PMI.	1
14	IMSKEACT2	PMI Mask EXTACT2 : When high, EXTACT2 will not trigger PMI.	1
15	IMSKEACT3	PMI Mask EXTACT3 : When high, EXTACT3 will not trigger PMI.	1

4.4.5 Heat Regulator Control Register			Configuration Index 005H
BIT	NAME	FUNCTION	DFLT
2:0	HTRGDLY<2:0>	Heat Regulator Delay: These bits determine the duration of time which the CPU is permitted to operate above the Heat Regulation Threshold before switching into Heat Regulation Mode to cool the CPU. HTRGDLY<2:0> — Heat Regulation Delay 0H — 16 seconds 1H — 32 seconds 2H — 1 minutes 3H — Reserved 4H — 2 minutes 5H — Reserved 6H — 4 minutes 7H — 8 minutes	0H
5:3	HTRGRAT<2:0>	Heat Regulator Ratio: These bits the regulation threshold above which the Heat Regulation Delay will begin counting, and they also define the worst case temperature that the Heat Regulator will impose as a maximum limit. This threshold is defined as a percentage of the worst case temperature for a given CPU. HTRGRAT<2:0> — Heat Regulation Threshold 0H — 50% 1H — 66% 2H — 80% 3H — 90% 4H — Reserved 5H — Reserved 6H — Reserved 7H — Reserved	0H
6	HTRGEN	Heat Regulator Enable: When high, the Heat Regulator will be enabled. When low, the system will never switch into Heat Regulation Mode. Please note that SLWCLKEN (index register 000H, bit 7) must be set to enable this feature. Also, SLCLK2SEL (index rgister 000H, bits 6:4) should be set to a value of 2H or higher.	0
7	HTRGLOCK	Heat Regulator Configuration Lock: When set high, register 5H bits 13:0 will be locked. This bit can only be written once.	0
9:8	Reserved		00
10	Reserved		0
11	Reserved		0
12	Reserved		0
13	Reserved		0
14	FRCSLWEN	Force SLOW Enable : When high, any high level on the FRCSLW/GPIO0 input pin will force the CPUCLK to slow speed. When low, the FRCSLW/GPIO0 pin will have the GPIO function.	0
15	FRCSLWLOCK	Force SLOW Lock : When high, bit 14 above (FRCSLWEN) will be locked. This bit can only be written once.	0

4.4.6 PMI Mask and Control Register			Configuration Index 006H
BIT	NAME	FUNCTION	DFLT
0	IMSKRW2PMI	Mask REDWOOD 2 source from PMI : When high, all the activity sources from REDWOOD 2 will not trigger a PMI. When low, it will.	1
1	IMSKLB	Mask Low Battery from PMI: When high, the LB inputs, LB, VLB, will not trigger a PMI. When low, they will.	1
2	IMSKSPNDTO	Mask Suspend Timeout from PMI: When high, the Suspend Mode Timeout will not trigger a PMI. When low, it will.	1
3	IMSKSLPTO	Mask Sleep Timeout from PMI: When high, Sleep Timeout will not trigger a PMI. Instead the Power Management Controller will change state directly from Doze to Sleep Mode.	1
4	IMSKDZTO	Mask Doze Timeout from PMI: When high, Doze Timeout will not trigger a PMI. Instead the Power Management Controller will change state directly from Fully-On to Doze Mode.	1
5	IMSKGENTO	Mask Generic Timeout from PMI: When high, Generic timeout will not trigger a PMI. When low, it will.	1
6	IMSKACTV	Mask Generic Activity from PMI: When high, Generic activity will not trigger a PMI. When low, it will.	1
7	IMSKPACTV	Mask Primary Activity from PMI: When high, Primary Activity will not trigger a PMI. When low, it will.	1
8	IMSKSACTV	Mask Secondary Activity from PMI: When high, Secondary activity will not trigger a PMI. When low, it will.	1
9	Reserved		1
10	IMSKSWSTBY	Mask SWTCH from PMI: When high, the SWTCH input will not trigger a PMI but makes the system into standby mode.	1
11	IMSKACPWR	Mask ACPWR from PMI: When high, the ACPWR input will not trigger a PMI. When low, either a rising or falling edge on the ACPWR input will trigger a PMI.	1
12	IMSKPROGTO	Mask Programmable Timeout Timer from PMI: When high, a timeout of the Programmable Timer will not trigger a PMI; when low it will.	1
13	IMSKGPTMR	Mask GP Timer from PMI: When high, a compare on the General Purpose Timer will not trigger a PMI; when low it will.	1
14	Reserved		1
15	Reserved		1

4.4.7 General Purpose Control Register			Configuration Index 007H
BIT	NAME	FUNCTION	DFLT
0	ACDISCNSRV	ACPWR Disable Conserve Mode: When high, and when ACPWR is high, Conserve Mode will be disabled. When low, ACPWR will not affect Conserve Mode.	0
1	ACON	ACPWR On: When high, ACPWR being high will force the Power Management Controller to Fully-On Mode. When low, ACPWR will not affect the Power Management Mode.	1

4:2	REFRPRD<2:0>	Refresh Period: These bits determine the refresh period for local DRAM. Bits<2:0> Refresh Period 0H 15uS 1H 30uS 2H 120uS 3H Reserved 4H Stopped 5H Reserved 6H Reserved 7H Reserved	0H
5	SLFREFEN	Self-Refresh Enable: When high, this bit enables self-refresh mode during Suspend Mode. In Fully-On, Conserve, Doze, or Sleep Mode refresh control will follow the timing selected by REFRPRD above. When low, Suspend Mode refresh will continue to be a CAS Before RAS refresh at the period selected by REFRPRD.	0
7:6	RINGS<1:0>	RINGS<1:0>: These bits indicate the number of pulses on the RING input that are required to validate a RING. Bits<1:0> RING's Required 0H Disabled 1H 1 2H 2 3H 4	0H
11:8	GPIODATA<3:0>	General Purpose I/O Data 3 to 0: When each bit's corresponding GPIODIR is low, a read of the bit returns the state of the GPIO pin, and a write has no effect. When GPIODIR is high, a read returns the value last written and a write sets the GPIO output to the value written.	0H
15:12	GPIODIR<3:0>	General Purpose I/O Direction 3 to 0: When low GPIO is an input pin. When high GPIO is an output pin.	0H

4.4.8 Stop Clock Control Register		Configuration Index 008H	
BIT	NAME	FUNCTION	DFLT
0	STPGLBEN	Stop Clock Global Enable: When high, an appropriate stop clock protocal will automatically be applied upon detection of any request to change the frequency of, or to stop, the CPU clock.	0
1	MORESTOP	More Stop: When high, and when STPGLBEN (bit 0 above) is also high, the CPU clock will be stopped upon detection of a Stop Grant cycle. When low, the CPU clock frequency will remain constant in the Stop Grant state. SLWCLKDIV set to STOPPED.	0
3:2	STPRELDLY<1:0>	STPCLK Release Delay (PLL Stablization Delay): This parameter defines the delay between restarting the CPU clock and de-asserting STPCLK. Bits<1:0> Delay 0H 0S 1H 1uS 2H 45uS 3H 1mS	0H

5:4	GRNTDLY<1:0>	STPCLK Latency Delay Select : Bits<1:0> — Latency Delay 0H — CPU Grant Bus Cycle 1H — 30uS 2H — 125uS 3H — 1mS	0H
6	WMSKINTR	Wake Mask INTR: When high, INTR will not restart the CPUCLK from a stop clock state. When low, any INTR will restart the CPUCLK.	1
7	WAIT4GRNT	Wait for Stop Grant: When high, any assertion of STPCLK will be held at least until a Stop Grant cycle is received. When low, STPCLK may be deasserted prior to a Stop Grant cycle.	0
8	Reserved		0
9	IOTRAPEN	I/O Trap Enable: When high, I/O cycles will be stretched as needed to ensure adequate SMI to RDY# setup time. When low, I/O trapping is still supported though under some circumstances SMI may not have adequate setup time.	0
10	Reserved		0
12:11	PCSTGSEL<1:0>	PC Staggering Select: Bits<1:0> — Stagger Period 0H — 240uS 1H — 4mS 2H — 16mS 3H — 64mS	0H
13	PCSTGDIS	PC Stagger Disable: When high, PC staggering is disabled but the stagger delay will still apply to LC timings.	0
14	PCSLWEN	PC Slow Enable: When high the CPUCLK will be switched to slow speed whenever any PC is in transition; when low, there will be no change in CPUCLK directly related to the PC's.	0
15	Reserved		0

4.4.9 Fully-On Mode Power Control Register — Configuration Index 009H

BIT	NAME	FUNCTION	DFLT
9:0	PCON<9:0>	Power Control Fully-On Mode 9 to 0: If any bit is high and Fully-On Mode is active, the corresponding PC pin will be active.	7H
10	GLBLPCEN	Global Power Control Enable: When high, all PC pins change state only when the Fully-On Mode Power Control Bits are toggled, regardless of power management modes. When low, PC pins follow the state of each Power Control Register by power management mode.	0
15:11	Reserved		0H

4.4.10 Doze Mode Power Control Register — Configuration Index 00AH

BIT	NAME	FUNCTION	DFLT
9:0	PCDZ<9:0>	Power Control Doze Mode 9 to 0: If any bit is high and Doze Mode is active, the corresponding PC pin will be active.	7H

10	SPNDDLY	Suspend Delay: When written high, the Power Management State latch will be held latched for 2 to 4mS thereafter. This can be used to delay entry to Suspend Mode. Writing the bit high triggers the latch but the bit will not be set high, and writing the bit low has no effect.	0
11	STRTDLY	Start Delays: When high, the CLKIN input will be internally latched for 30 to 60mS following each resume. When low, the internal CLK will immediately follow CLKIN upon any resume.	0
12	Reserved		0
14:13	Reserved		0H
15	Reserved		0

4.4.11 Sleep Mode Power Control Register — Configuration Index 00BH

BIT	NAME	FUNCTION	DFLT
9:0	PCSLP<9:0>	Power Control Sleep Mode 9 to 0: If any bit is high and Sleep Mode is active, the corresponding PC pin will be active.	7H
10	LBLEDFLSH	Low Battery LED Flasher Enable: When high, output pin PC6 will be enabled to function as an LED flasher output. This output may be used to indicate Low Battery Status or any other system status desired.	0
12:11	LBFLSHRAT<1:0>	Low Battery LED Flash Rate Selects <1:0>: These bits control the flash rate of the Low Battery LED Flasher output while LBLEDFLSH is high. LBFLSHRAT<1:0> — LED Flash Rate 0H — 0.5Hz 1H — 1Hz 2H — 2Hz 3H — 4Hz	0H
14:13	LBFLSHDUR<1:0>	Low Battery LED Flash Duration: These bits control the duration of the Low Battery Flasher pulses while LBLEDFLSH (bit 10 above) is high. LBFLSHDUR<1:0> — Flash Duration 0H — 256mS 1H — 128mS 2H — 62.5mS 3H — 31.25mS **Note: When the flash rate is 2H, the flash duration can not be set to 0H. And when the flash rate is 3H, the flash duration can not be set to 0H or 1H.**	0H
15	VLBFLSHEN	Very Low Battery Flash Enable: When high, the Low Battery Flasher, will automatically flash at a rate of 1Hz whenever the LB input is high or at a rate of 4Hz whenever the VLB input is high.	0

4.4.12 Suspend Mode Power Control Register — Configuration Index 00CH

BIT	NAME	FUNCTION	DFLT
9:0	PCSPND<9:0>	Power Control Suspend Mode 9 to 0: If any bit is high and Suspend Mode is active, the corresponding PC pin will be active.	7H

10	SPLEDFLSH	Suspend LED Flasher Enable: When high, output pin PC5 will be enabled to function as an LED flasher output.	0
12:11	SPFLSHRAT<1:0>	Suspend LED Flash Rate Selects <1:0>: These bits control the flash rate of the Suspend LED Flasher output (PC5) while SPLEDFLSH is high. SPFLSHRAT<1:0> — LED Flash Rate 0H — 0.5Hz 1H — 1Hz 2H — 2Hz 3H — 4Hz	0H
14:13	SPFLSHDUR<1:0>	Suspend LED Flash Duration: These bits control the duration of the Suspend Flasher pulses while SPLEDFLSH (bit 10 above) is high. SPFLSHDUR<1:0> — Flash Duration 0H — 256mS 1H — 128mS 2H — 62.5mS 3H — 31.25mS **Note: When the flash rate is 2H, the flash duration can not be set to 0H. And when the flash rate is 3H, the flash duration can not be set to 0H or 1H.**	0H
15	Reserved		0

4.4.13 Timer Register — Configuration Index 00DH

BIT	NAME	FUNCTION	DFLT
3:0	GENTMR<3:0>	Generic Timer, 3 to 0: Bits<3:0> Timeout — Bits<3:0> Timeout 0H Disabled — 8H 25 Seconds 1H 2 Seconds — 9H 30 Seconds 2H 4 Seconds — AH 40 Seconds 3H 6 Seconds — BH 50 Seconds 4H 8 Seconds — CH 60 Seconds 5H 10 Seconds — DH 75 Seconds 6H 15 Seconds — EH 90 Seconds 7H 20 Seconds — FH 120 Seconds	0H
6:4	SPNDTMR<2:0>	Suspend Mode Timer, 2 to 0: Bits<2:0> Timeout — Bits<2:0> Timeout 000 Disabled — 100 20 Minutes 001 5 Minutes — 101 30 Minutes 010 10 Minutes — 110 40 Minutes 011 15 Minutes — 111 60 Minutes	0H
9:7	SLPTMR<2:0>	Sleep Mode Timer, 2 to 0: Bits<2:0> Timeout — Bits<2:0> Timeout 000 Disabled — 100 6 Minutes 001 1 Minute — 101 8 Minutes 010 2 Minutes — 110 12 Minutes 011 4 Minutes — 111 16 Minutes	0H

12:10	DZTMR<2:0>	Doze Mode Timer, 2 to 0: Bits<2:0> Timeout Bits<2:0> Timeout 000 Disabled 100 1 Second 001 .125 Seconds 101 4 Seconds 010 .250 Seconds 110 8 Seconds 011 .500 Seconds 111 16 Seconds	0H
15:13	Reserved		0

4.4.14 PMC Miscellaneous Control Register 1 | Configuration Index 00EH

BIT	NAME	FUNCTION	DFLT
0	Reserved		0
1	Reserved		0
3:2	GPCTSEL<1:0>	General Purpose Counter/Timer Select: Bits<1:0> Function 00 16 Bit Counter 01 24 Bit Counter 10 1 Second Timer 11 1 Minute Timer When either Counter is enabled, GPIO3 will be enabled as the counter clock. When the 1 Second Timer is enabled, a 1HZ clock will be enabled, and when the 1 Minute Timer is enabled, a 1 Minute clock will be enabled. The status of the Counter/Timer may be read at register 10H	0H
4	GPCTEN	General Purpose Counter/Timer Enable: When high, the General Purpose Counter/Timer will be enabled; when low it will be disabled.	0
5	WMSKVLBNAC	Wake Mask VLB if Not ACPWR: When high, VLB input being high with ACPWR low will inhibit any wake-up from Suspend or Standby modes; when low, VLB will not affect the wake-up mechanism.	0
6	WAKE0MSK	Wake0 Mask : When high, the WAKE0 input will not trigger a wake-up from Suspend or Standby modes; when low it will.	1
7	WAKE1MSK	Wake1 Mask : When high, the WAKE1 input will not trigger a wake-up from Suspend or Standby modes; when low it will.	1
8	WMSKRING	Wake Mask RING: When high, the RING input will not trigger a wake-up from Suspend or Standby modes; when low it will.	1
9	WMSKRTC	Wake Mask RTC: When high, the RTC input will not trigger a wake-up from Suspend or Standby modes; when low it will.	1
10	Reserved		X
11	WMSKTMR	Wake Mask GP Timer: When high, a compare on the GP Timer will not trigger a wake-up from Suspend or Standby modes; when low it will.	1
15:12	PRDCTID<3:0>	Product Identification: These four bits identify the product and revision. FH = REDWOOD. These bits are read-only.	FH

4.4.15 Reserved			Configuration Index 00FH
BIT	NAME	FUNCTION	DFLT
4:0	Reserved		0H
15:5	Reserved		000H

4.4.16 GP Counter/Timer Register			Configuration Index 010H
BIT	NAME	FUNCTION	DFLT
15:0	GPCT<15:0>	General Purpose Counter/Timer, 15 to 0: Reading this register returns the current value of the General Purpose Counter/Timer. When the 24 bit counter is enabled these bits represent counter bits 23:8; otherwise they represent counter/timer bits 15:0. Any write to this register will reset the entire counter/timer.	0000H

4.4.17 GP Timer Compare Register			Configuration Index 011H
BIT	NAME	FUNCTION	DFLT
15:0	GPTMRCMP<15:0>	These bits represent a compare value at which the General Purpose Counter/Timer will trigger an interrupt if the corresponding PMI is unmasked.	0000H

4.4.18 Debounce Control Register			Configuration Index 012H
BIT	NAME	FUNCTION	DFLT
0	DBDIS0	Debounce Disable 0: When low, ACPWR and SWITCH are debounced from 15-23mS. When high, they will have no debounce.	0
1	Reserved		0
2	DBDIS1	Debounce Disable 1: When low, the debounce circuits for LB and VLB are enabled. The debounce duration will be determined by register 012H, bit3. When high, they will have no debounce.	0
3	DBTMDR1	Debounce Time Duration 1 : When low, LB and VLB are debounced from 15-23mS. When high, it will be 10 seconds. Please note that DBDIS1 (register 012H bit 2) must be set low to enable this feature.	0
4	DBDIS2	Debounce Disable 2: When low, the debounce circuits for EXTACT0 and EXTACT1 are enabled. The debounce duration will be determined by register 012H, bit5. When high, they will have no debounce.	0
5	Reserved		0
6	DBDIS3	Debounce Disable 3: When low, the debounce circuits for EXTACT2 and EXTACT3 are enabled. The debounce duration will be determined by register 012H, bit7. When high, they will have no debounce.	0
7	Reserved		0
11:8	Reserved		XH

12	WAKE0DBDIS	Wake0 Debounce Disable : When low, the debounce circuit for Wake0 is enabled. The debounce duration will be determined by register 012H, bit13. When high, they will have no debounce.	0
13	Reserved		0
14	WAKE1DBDIS	Wake1 Debounce Disable : When low, the debounce circuit for Wake0 is enabled. The debounce duration will be determined by register 012H, bit15. When high, they will have no debounce.	0
15	Reserved		0

4.4.19 PMC Miscellaneous Control Register 2		Configuration Index 013H	
BIT	NAME	FUNCTION	DFLT
0	Reserved		0
1	SMIRDYEN	SMIRDY# Enable: When high, and SMISEL (index register 103H, bit 9) is high, SMIRDY# will terminate any SMIADS# initiated cycle. When low, and SMISEL is high, both SMIADS# and ADS# initiated cycles will be terminated by RDY#.	1
2	PWRGDSTBYDIS	PowerGood Standby Disable : When low, falling edge of PWRGOOD input will trigger standby mode. When high, it will have no effect.	0
3	GLBLRSTEN	Global Reset Enable : When high, all the logic will be reset (except internal RTC) when PowerGood makes a transition from low to high. When low, internal RTC and PMU logic will not be reset when PowerGood makes a transition.	0
4	PMCRSTEN	PMC Reset Enable: When high, PMU registers will be reset on RCRST# or SPNDNRST. When low, PMC registers will be reset on RCRST# only.	0
5	Reserved		0
6	Reserved		0
7	Reserved		0
8	Reserved		0
9	WAKE0TOGL	WAKE0 Toggle Select : When low, only rising edge of WAKE0 input will trigger PMI and Wake function. When high, both rising and falling edges will trigger PMI and Wake function.	0
10	WAKE1TOGL	WAKE1 Toggle Select : When low, only rising edge of WAKE1 input will trigger PMI and Wake function. When high, both rising and falling edges will trigger PMI and Wake function.	0
11	Reserved		0
12	Reserved		0
14:13	Reserved		0
15	RSTCPUFLG	RSTCPU Flag: When high, this bit indicates that a RSTCPU has occured. It can be reset by writing it low.	0

4.4.20 Optional GPIO Control Register 2			Configuration Index 014H
BIT	NAME	FUNCTION	DFLT
1:0	GPIOADATA<1:0>	General Purpose I/O A Data 1 to 0: When each bit's corresponding GPIODIR is low, a read of the bit returns the state of the GPIO pin, and a write has no effect. When GPIODIR is high, a read returns the value last written and a write sets the GPIO output to the value written. Note : These bits must be used with index register 110H, bits <12:11>.	00
3:2	GPIOADIR<1:0>	General Purpose I/O A Direction 1 to 0 When low GPIO is an input pin. When high GPIO is an output pin. Note : These bits must be used with index register 110H, bits <12:11>.	00
5:4	GPIOBDATA<1:0>	General Purpose I/O B Data 1 to 0: When each bit's corresponding GPIODIR is low, a read of the bit returns the state of the GPIO pin, and a write has no effect. When GPIODIR is high, a read returns the value last written and a write sets the GPIO output to the value written. Note : These bits must be used with index register 111H, bit7 and bit 5	00
7:6	GPIOBDIR<1:0>	General Purpose I/O B Direction 1 to 0 When low GPIO is an input pin. When high GPIO is an output pin. Note : These bits must be used with index register 111H, bit 7 and bit 5.	00
9:8	GPIOCDATA<1:0>	General Purpose I/O C Data 1 to 0: When each bit's corresponding GPIODIR is low, a read of the bit returns the state of the GPIO pin, and a write has no effect. When GPIODIR is high, a read returns the value last written and a write sets the GPIO output to the value written. Note : These bits must be used with index register 111H, bit 11 and 110H, bit 8.	00
11:10	GPIOCDIR<1:0>	General Purpose I/O C Direction 1 to 0 When low GPIO is an input pin. When high GPIO is an output pin. Note : These bits must be used with index register 111H, bit 11 and 110H, bit 8	00
15:12	Reserved		XH

4.4.21 Leakage Control Register			Configuration Index 015H
BIT	NAME	FUNCTION	DFLT
0	Reserved		0
1	DRAMLCDIS	DRAM Interface leakage control disable : 0 = Enabled. 1 = Disabled.	0
2	Reserved		0
3	Reserved		0
4	Reserved		0
5	GPIOLCDIS	GPIO Interface leakage control disable : 0 = Enabled. 1 = Disabled.	0
6	PC49LCDIS	PC 4 to PC 9 Interface leakage control disable : 0 = Enabled. 1 = Disabled.	0
7	Reserved		0

8	BMLCDIS	Battery Management Inputs (LB, VLB, ACPWR) leakage control disable : 0 = Enabled, 1= Disabled.	0
11:9	Reserved		XH
11:10	Reserved		XX
13:12	Reserved		XX
14	Reserved		0
15	LCDIS	Leakage Control Disable: When high, no leakage control circuitry will be engaged upon entering Suspend Mode. When low, leakage control will automatically be engaged on entering Suspend Mode.	0

4.4.22 Reserved		Configuration Index 016H	
BIT	NAME	FUNCTION	DFLT
3:0	Reserved		XH
7:4	Reserved		XH
11:8	Reserved		XH
15:12	Reserved		XH

4.4.23 Reserved		Configuration Index 017H	
BIT	NAME	FUNCTION	DFLT
3:0	Reserved		XH
7:4	Reserved		XH
11:8	Reserved		XH
15:12	Reserved		XH

4.4.24 Reserved		Configuration Index 018H	
BIT	NAME	FUNCTION	DFLT
3:0	Reserved		XH
7:4	Reserved		XH
11:8	Reserved		XH
15:12	Reserved		XH

4.4.25 Secondary Activity Mask Register		Configuration Index 019H	
BIT	NAME	FUNCTION	DFLT
0	SAMSKVID	Secondary Activity Mask Video Accesses: When high Video accesses will not trigger the Secondary Idle Detector.	1
2:1	Reserved		XX
3	SAMSKKBD	Secondary Activity Mask Keyboard Accesses: When high Keyboard access will not trigger the Secondary Idle Detector.	1
5:4	Reserved		1

6	SAMSKPROG0	Secondary Activity Mask Programmable Range 0 : When high, any access to the programmable range 0 will not trigger the Secondary Idle Detector.	1
7	SAMSKPROG1	Secondary Activity Mask Programmable Range 1 : When high, any access to the programmable range 1 will not trigger the Secondary Idle Detector.	1
8	SAMSKPROG2	Secondary Activity Mask Programmable Range 2 : When high, any access to the programmable range 2 will not trigger the Secondary Idle Detector.	1
9	SAMSKPROG3	Secondary Activity Mask Programmable Range 3 : When high, any access to the programmable range 3 will not trigger the Secondary Idle Detector.	1
11:10	Reserved		XX
12	SAMSKEACT0	Secondary Activity Mask EXTACT0 : When high, EXTACT0 will not trigger the Secondary Idle Detector.	1
13	SAMSKEACT1	Secondary Activity Mask EXTACT1 : When high, EXTACT1 will not trigger the Secondary Idle Detector.	1
14	SAMSKEACT2	Secondary Activity Mask EXTACT2 : When high, EXTACT2 will not trigger the Secondary Idle Detector.	1
15	SAMSKEACT3	Secondary Activity Mask EXTACT3 : When high, EXTACT3 will not trigger the Secondary Idle Detector.	1

4.4.26 Additional Activity Source Register — Configuration Index 01AH

BIT	NAME	FUNCTION	DFLT
0	WAKE0ACTV	WAKE0 Active : When WAKE0 input is detected high, this bit will be set high. This bit is read only, but will be cleared on any write to this register.	0
1	WAKE1ACTV	WAKE1 Active : When WAKE1 input is detected high, this bit will be set high. This bit is read only, but will be cleared on any write to this register.	0
2	INTRACTV	Interrupt Active : Whenever a CPU interrupt request is detected, this bit will be set high. This bit is read only, but will be cleared on any write to this register.	0
3	Reserved		0
4	DZTO	Doze Timeout Status: When high, this bit indicates that a Doze Timeout has occured. This bit will remain active until Primary Activity is detected, or until it is written low. Writing this bit high has no effect.	0
5	SLPTO	Sleep Timeout Status: When high, this bit indicates that a Sleep Timeout has occured. This bit will remain active until Primary Activity is detected, or until it is written low. Writing this bit high has no effect.	0
6	SPNDTO	Suspend Timeout Status: When high, this bit indicates that a Suspend Timeout has occured. This bit will remain active until Primary Activity is detected, or until it is written low. Writing this bit high has no effect.	0
7	GENTO	Generic Timer Timeout: When high, this bit indicates that a Generic Timer Timeout has occured. This bit will remain active until Primary Activity is detected, or until it is written low. Writing this bit high has no effect.	0

8	PRTMR0TO	Programmable timeout timer 0 Timeout Status : When the Programmable timeout timer 0 (register 028H) timeout occurs, this bit will be set high. This bit remains low until a reset of the timer occurs or until it is written low. Writing this bit high has no effect.	0
9	PRTMR1TO	Programmable timeout timer 1 Timeout Status : When the Programmable timeout timer 1 (register 029H) timeout occurs, this bit will be set high. This bit remains low until a reset of the timer occurs or until it is written low. Writing this bit high has no effect.	0
10	PRTMR2TO	Programmable timeout timer 2 Timeout Status : When the Programmable timeout timer 2 (register 02AH) timeout occurs, this bit will be set high. This bit remains low until a reset of the timer occurs or until it is written low. Writing this bit high has no effect.	0
11	PRTMR3TO	Programmable timeout timer 3 Timeout Status : When the Programmable timeout timer 3 (register 02BH) timeout occurs, this bit will be set high. This bit remains low until a reset of the timer occurs or until it is written low. Writing this bit high has no effect.	0
12	PRTOPMI0	**Programmable timeout timer 0 PMI Flag : When high, a PMI has been triggered by programmable timeout timer 0. When low, no PMI has been triggered by programmable timeout timer 0.** This bit must be written low after resetting the PMI source bits in index register 001H.	0
13	PRTOPMI1	**Programmable timeout timer 1 PMI Flag : When high, a PMI has been triggered by programmable timeout timer 1. When low, no PMI has been triggered by programmable timeout timer 1.** This bit must be written low after resetting the PMI source bits in index register 001H.	0
14	PRTOPMI2	**Programmable timeout timer 2 PMI Flag : When high, a PMI has been triggered by programmable timeout timer 2. When low, no PMI has been triggered by programmable timeout timer 2.** This bit must be written low after resetting the PMI source bits in index register 001H.	0
15	PRTOPMI3	**Programmable timeout timer 3 PMI Flag : When high, a PMI has been triggered by programmable timeout timer 3. When low, no PMI has been triggered by programmable timeout timer 3.** This bit must be written low after resetting the PMI source bits in index register 001H.	0

4.4.27 Additional Primary Activity Mask Register		Configuration Index 01BH	
BIT	NAME	FUNCTION	DFLT
0	PAMSKWAKE0	Primary Activity Mask WAKE0 : When high, WAKE0 will not trigger the Primary Idle Detector.	1
1	PAMSKWAKE1	Primary Activity Mask WAKE1 : When high, WAKE1 will not trigger the Primary Idle Detector.	1
2	PAMSKINTR	Primary Activity Mask INTR: When high, INTR will not trigger the Primary Idle Detector.	1
3	PAMSKPMI	Primary Activity Mask PMI: When high, PMI will not trigger the Primary Idle Detector.	1
4	PAMSKHOLD	Primary Activity Mask HOLD Request: When high CPU Hold Request will not trigger the Primary Idle Detector.	1

5	PAMSKNMI	Primary Activity Mask NMI: When high, NMI will not trigger the Primary Idle Detector.	1
6	PAMSKDMA	Primary Activity Mask DMA : When high. ISA DMA will not trigger the Primary Idle Detector.	1
7	PAMSKMSTR	Primary Activity Mask MASTER: When high. ISA MASTER will not trigger the Primary Idle Detector.	1
10:8	Reserved		XXX
11	Reserved		0
13:12	Reserved		XX
14	HD2EN	Hard Disk Secondary Enable : If high, any access to both primary and secondary drives will trigger hard disk activity. If low, only the primary drive will be selected.	0
15	Reserved	.	1

4.4.28 Additional Secondary Activity Control Register | Configuration Index 01CH

BIT	NAME	FUNCTION	DFLT
0	SAMSKWAKE0	Secondary Activity Mask WAKE0 : When high, WAKE0 will not trigger the Secondary Idle Detector. When low, it will.	1
1	SAMSKWAKE1	Secondary Activity Mask WAKE1 : When high, WAKE1 will not trigger the Secondary Idle Detector. When low, it will.	1
2	SAMKSINTR	Secondary Activity Mask INTR : When high. INTR will not trigger the Secondary Idle Detector. When low, it will.	1
3	SAMSKPMI	Secondary Activity Mask PMI : When high. PMI will not trigger the Secondary Idle Detector. When low, it will.	1
4	SAMSKIRQ0	Secondary Activity Mask IRQ0 : When high. Timer Interrupt IRQ0 will not trigger the Secondary Idle Detector. When low, it will.	1
5	Reserved		X
6	SAMSKDMA	Secondary Activity Mask DMA : When high. ISA DMA will not trigger the Secondary Idle Detector. When low, it will.	1
7	SAMSKMSTR	Secondary Activity Mask MASTER: When high. ISA MASTER will not trigger the Secondary Idle Detector. When low, it will.	1
8	Reserved	.	0
11:9	SACTVTMR<2:0>	Secondary Activity Timer, bits <2:0>: These bits determine how long the CPU will be returned to high speed following detection of Secondary Activity.	4H

Bits<2:0>	Timeout	Bits<2:0>	Timeout
0H	125uS	4H	8mS
1H	1mS	5H	16mS
2H	2mS	6H	32mS
3H	4mS	7H	64mS

12	Reserved		X
13	Reserved		0
14	Reserved		0
15	Reserved		1

4.4.29 Additional PMI Mask Register		Configuration Index 01DH	
BIT	NAME	FUNCTION	DFLT
0	IMSKWAKE0	Mask WAKE0 from PMI : When high, WAKE0 will not trigger a PMI. When low, it will.	1
1	IMSKWAKE1	Mask WAKE1 from PMI : When high, WAKE1 will not trigger a PMI. When low, it will.	1
2	Reserved		X
3	IMSKRTC	Mask RTC from PMI : When high, RTC interrupt will not trigger a PMI. When low, it will.	1
5:4	RESCHED<1:0>	Reschedule PMI: When either of these bits are set high, a PMI will be triggered every N miliseconds as indicated below. Bits<1:0> — Rescheduled Every 0H — Disabled 1H — 64mS 2H — 256mS 3H — 1S	0H
6	SFTSMI	Soft SMI: When low, writing one to this bit will trigger an immediate SMI but will not toggle the bit. This bit may only be set high by back to back writes, first setting the bit to low, then setting it to high. When this bit is set high any write to port B0H will trigger an immediate SMI. Once the bit has been set high a single write to low will reset it low.	0
7	Reserved		X
8	IMSKPRTMR0TO	Mask Programmable timeout timer 0 (register 028H) Timeout from PMI : When high, Programmable timeout timer 0 Timeout will not trigger a PMI. When low, it will.	1
9	IMSKPRTMR1TO	Mask Programmable timeout timer 1 (register 029H) Timeout from PMI : When high, Programmable timeout timer 1 Timeout will not trigger a PMI. When low, it will.	1
10	IMSKPRTMR2TO	Mask Programmable timeout timer 2 (register 02AH) Timeout from PMI : When high, Programmable timeout timer 2 Timeout will not trigger a PMI. When low, it will.	1
11	IMSKPRTMR3TO	Mask Programmable timeout timer 3 (register 02BH) Timeout from PMI : When high, Programmable timeout timer 3 Timeout will not trigger a PMI. When low, it will.	1
15:12	Reserved		XH

4.4.30 Miscellaneous Control Register		Configuration Index 01EH	
BIT	NAME	FUNCTION	DFLT
0	PMIFLGEN	PMI Flag Enable : 0 = Disabled. 1 = Enabled.	1
1	PAFLGEN	Primary Activity Flag Enable : 0 = Disabled. 1 = Enabled.	0
2	SAFLGEN	Secondary Activity Flag Enable : 0 = Disabled. 1 = Enabled.	0
7:3	Reserved		XH
11:8	Reserved		XH
13:12	Reserved		XX
14	Reserved		0
15	Reserved		0

4.4.31 REDWOOD 1 Identification Register			Configuration Index 01FH
BIT	NAME	FUNCTION	DFLT
3:0	R1ID<3:0>	REDWOOD 1 Revision number ID <3:0> : 0H = Initial Revision. 1H = A-step silicon. These bits are read only.	1H
15:4	Reserved		XXXH

4.4.32 Programmable Range Compare Register 0			Configuration Index 020H
BIT	NAME	FUNCTION	DFLT
9:0	PRMA0<9:0>	Programmable Range Monitor 0 Addresses <9:0>: These bits represent the values to be compared against appropriate CPU addresses. For an I/O Monitor the addresses monitored will be A<9:0>, and for a Memory Monitor they will be A<23:14>.	00H
13:10	Reserved		0
14	PROSHDW0EN	Programmable Shadow Register 0 Enable : 0 = Disabled. 1 = Enabled, This register will be used as a pointer to an IO register for shadowing. The contents of the IO register being shadowed can be read from low byte of index register 080H.	0
15	PROCS0EN	Programmable Chip Select 0 Enable : 0 = Disabled. 1 = Enabled, This register will be used for GPCS0#.	0

4.4.33 Programmable Range Compare Register 0			Configuration Index 021H
BIT	NAME	FUNCTION	DFLT
9:0	PRMCMPEN0<9:0>	Programmable Range Monitor 0 Compare Enable <9:0>: These bits indicate which of the Programmable Range Monitor Addresses (index register 020H) will be compared against the equivalent CPU Address. For an I/O Compare they enable A<9:0>, and for a Memory Compare they enable A<23:14>. When high, the equivalent address will be compared, when low it will be ignored.	00H
10	PRMWR0EN	Programmable Range Monitor 0 Write Enable: When high, the Monitor will select write cycles.	0
11	PRMRD0EN	Programmable Range Monitor 0 Read Enable: When high, the Monitor will select read cycles.	0
12	PRM0MIO	Programmable Range Monitor 0 Memory or I/O Compare Enable: When high, the Monitor will select memory addresses, and when low the Monitor will select I/O addresses.	0
13	PRM0EN	Programmable Range Monitor 0 Enable: When high, the Programmable Range Monitor 0 will be enabled.	0
15:14	Reserved		00

4.4.34 Programmable Range Compare Register 1		Configuration Index 022H	
BIT	NAME	FUNCTION	DFLT
9:0	PRMA1<9:0>	Programmable Range Monitor 1 Addresses <9:0>: These bits represent the values to be compared against appropriate CPU addresses. For an I/O Monitor the addresses monitored will be A<9:0>, and for a Memory Monitor they will be A<23:14>.	00H
13:10	Reserved		0
14	PROSHDW1EN	Programmable Shadow Register 1 Enable : 0 = Disabled. 1 = Enabled, This register will be used as a pointer to an IO register for shadowing. The contents of the IO register being shadowed can be read from high byte of index register 080H.	0
15	PROCS1EN	Programmable Chip Select 1 Enable : 0 = Disabled. 1 = Enabled, This register will be used for GPCS1#.	0

4.4.35 Programmable Range Compare Register 1		Configuration Index 023H	
BIT	NAME	FUNCTION	DFLT
9:0	PRMCMPEN1<9:0>	Programmable Range Monitor 1 Compare Enable <9:0>: These bits indicate which of the Programmable Range Monitor Addresses (index register 022H) will be compared against the equivalent CPU Address. For an I/O Compare they enable A<9:0>, and for a Memory Compare they enable A<23:14>. When high, the equivalent address will be compared, when low it will be ignored.	00H
10	PRMWR1EN	Programmable Range Monitor 1 Write Enable: When high, the Monitor will select write cycles.	0
11	PRMRD1EN	Programmable Range Monitor 1 Read Enable: When high, the Monitor will select read cycles.	0
12	PRM1MIO	Programmable Range Monitor 1 Memory or I/O Compare Enable: When high, the Monitor will select memory addresses, and when low the Monitor will select I/O addresses.	0
13	PRM1EN	Programmable Range Monitor 1 Enable: When high, the Programmable Range Monitor 1 will be enabled.	0
15:14	Reserved		00

4.4.36 Programmable Range Compare Register 2		Configuration Index 024H	
BIT	NAME	FUNCTION	DFLT
9:0	PRMA2<9:0>	Programmable Range Monitor 2 Addresses <9:0>: These bits represent the values to be compared against appropriate CPU addresses. For an I/O Monitor the addresses monitored will be A<9:0>, and for a Memory Monitor they will be A<23:14>.	00H
13:10	Reserved		0
14	PROSHDW2EN	Programmable Shadow Register 2 Enable : 0 = Disabled. 1 = Enabled, This register will be used as a pointer to an IO register for shadowing. The contents of the IO register being shadowed can be read from low byte of index register 081H.	0
15	PROCS2EN	Programmable Chip Select 2 Enable : 0 = Disabled. 1 = Enabled, This register will be used for GPCS2#.	0

4.4.37 Programmable Range Compare Register 2		Configuration Index 025H	
BIT	NAME	FUNCTION	DFLT
9:0	PRMCMPEN2<9:0>	Programmable Range Monitor 2 Compare Enable <9:0>: These bits indicate which of the Programmable Range Monitor Addresses (index register 024H) will be compared against the equivalent CPU Address. For an I/O Compare they enable A<9:0>, and for a Memory Compare they enable A<23:14>. When high, the equivalent address will be compared, when low it will be ignored.	00H
10	PRMWR2EN	Programmable Range Monitor 2 Write Enable: When high, the Monitor will select write cycles.	0
11	PRMRD2EN	Programmable Range Monitor 2 Read Enable: When high, the Monitor will select read cycles.	0
12	PRM2MIO	Programmable Range Monitor 2 Memory or I/O Compare Enable: When high, the Monitor will select memory addresses, and when low the Monitor will select I/O addresses.	0
13	PRM2EN	Programmable Range Monitor 2 Enable: When high, the Programmable Range Monitor 2 will be enabled.	0
15:14	Reserved		00

4.4.38 Programmable Range Compare Register 3		Configuration Index 026H	
BIT	NAME	FUNCTION	DFLT
9:0	PRMA3<9:0>	Programmable Range Monitor 3 Addresses <9:0>: These bits represent the values to be compared against appropriate CPU addresses. For an I/O Monitor the addresses monitored will be A<9:0>, and for a Memory Monitor they will be A<23:14>.	00H
13:10	Reserved		0
14	PROSHDW3EN	Programmable Shadow Register 3 Enable : 0 = Disabled. 1 = Enabled, This register will be used as a pointer to an IO register for shadowing. The contents of the IO register being shadowed can be read from high byte of index register 081H.	0
15	PROCS3EN	Programmable Chip Select 3 Enable : 0 = Disabled. 1 = Enabled, This register will be used for GPCS3#.	0

4.4.39 Programmable Range Compare Register 3		Configuration Index 027H	
BIT	NAME	FUNCTION	DFLT
9:0	PRMCMPEN3<9:0>	Programmable Range Monitor 3 Compare Enable <9:0>: These bits indicate which of the Programmable Range Monitor Addresses (index register 026H) will be compared against the equivalent CPU Address. For an I/O Compare they enable A<9:0>, and for a Memory Compare they enable A<23:14>. When high, the equivalent address will be compared, when low it will be ignored.	00H
10	PRMWR3EN	Programmable Range Monitor 3 Write Enable: When high, the Monitor will select write cycles.	0
11	PRMRD3EN	Programmable Range Monitor 3 Read Enable: When high, the Monitor will select read cycles.	0

12	PRM3MIO	Programmable Range Monitor 3 Memory or I/O Compare Enable: When high, the Monitor will select memory addresses, and when low the Monitor will select I/O addresses.	0
13	PRM3EN	Programmable Range Monitor 3 Enable: When high, the Programmable Range Monitor 3 will be enabled.	0
15:14	Reserved		00

4.4.40 Programmable Timeout Timer Register 0 — Configuration Index 028H

BIT	NAME	FUNCTION	DFLT
3:0	PROGTMR0<3:0>	Programmable Timeout Timer 0 , Bits 3 to 0: Bits<3:0> Timeout — Bits<3:0> Timeout 0H Reserved — 8H 2 Minutes 1H 5 Seconds — 9H 3 Minutes 2H 10 Seconds — AH 4 Minutes 3H 15 Seconds — BH 6 Minutes 4H 30 Seconds — CH 8 Minutes 5H 45 Seconds — DH 10 Minutes 6H 60 Seconds — EH 15 Minutes 7H 90 Seconds — FH 20 Minutes	0H
6:4	Reserved		000
7	TMR0SOURCE	Clock Source for the Programmable Timeout Timer 0 : 0 = Use internal clock source. 1 = Use EXTACT0 as the clock source.	0
13:8	Reserved		XH
14	TMR0PC2EN	Timeout Timer 0 To PC2 Enable : If high, when the programmable timer 0 times out, it will set PC2 low.	0
15	TMR0EN	Programmable Timer 0 Enable : 0 = The programmable timeout timer is disabled (stopped). 1 = The programmable timeout timer is enabled.	0

4.4.41 Programmable Timeout Timer Register 1 — Configuration Index 029H

BIT	NAME	FUNCTION	DFLT
3:0	PROGTMR1<3:0>	Programmable Timeout Timer 1 , Bits 3 to 0: Bits<3:0> Timeout — Bits<3:0> Timeout 0H Reserved — 8H 2 Minutes 1H 5 Seconds — 9H 3 Minutes 2H 10 Seconds — AH 4 Minutes 3H 15 Seconds — BH 6 Minutes 4H 30 Seconds — CH 8 Minutes 5H 45 Seconds — DH 10 Minutes 6H 60 Seconds — EH 15 Minutes 7H 90 Seconds — FH 20 Minutes	0H
6:4	Reserved		000
7	TMR1SOURCE	Clock Source for the Programmable Timeout Timer 1 : 0 = Use internal clock source. 1 = Use EXTACT1 as the clock source.	0
13:8	Reserved		XH

14	TMR1PC3EN	Timeout Timer 1 To PC3 Enable : If high, when the programmable timer 1 times out, it will set PC3 low.	0
15	TMR1EN	Programmable Timer 1 Enable : 0 = The programmable timeout timer is disabled (stopped). 1 = The programmable timeout timer is enabled.	0

4.4.42 Programmable Timeout Timer Register 2 — Configuration Index 02AH

BIT	NAME	FUNCTION	DFLT
3:0	PROGTMR2<3:0>	Programmable Timeout Timer 2 , Bits 3 to 0:	0H
6:4	Reserved		000
7	TMR2SOURCE	Clock Source for the Programmable Timeout Timer 2 : 0 = Use internal clock source. 1 = Use EXTACT2 as the clock source.	0
13:8	Reserved		XH
14	TMR2PC8EN	Timeout Timer 2 To PC8 Enable : If high, when the programmable timer 2 times out, it will set PC8 low.	0
15	TMR2EN	Programmable Timer 2 Enable : 0 = The programmable timeout timer is disabled (stopped). 1 = The programmable timeout timer is enabled.	0

Bits<3:0>	Timeout	Bits<3:0>	Timeout
0H	Reserved	8H	2 Minutes
1H	5 Seconds	9H	3 Minutes
2H	10 Seconds	AH	4 Minutes
3H	15 Seconds	BH	6 Minutes
4H	30 Seconds	CH	8 Minutes
5H	45 Seconds	DH	10 Minutes
6H	60 Seconds	EH	15 Minutes
7H	90 Seconds	FH	20 Minutes

4.4.43 Programmable Timeout Timer Register 3 — Configuration Index 02BH

BIT	NAME	FUNCTION	DFLT
3:0	PROGTMR3<3:0>	Programmable Timeout Timer 3 , Bits 3 to 0:	0H
6:4	Reserved		000
7	TMR3SOURCE	Clock Source for the Programmable Timeout Timer 3 : 0 = Use internal clock source. 1 = Use EXTACT3 as the clock source.	0
13:8	Reserved		XH

Bits<3:0>	Timeout	Bits<3:0>	Timeout
0H	Reserved	8H	2 Minutes
1H	5 Seconds	9H	3 Minutes
2H	10 Seconds	AH	4 Minutes
3H	15 Seconds	BH	6 Minutes
4H	30 Seconds	CH	8 Minutes
5H	45 Seconds	DH	10 Minutes
6H	60 Seconds	EH	15 Minutes
7H	90 Seconds	FH	20 Minutes

14	TMR3PC9EN	Timeout Timer 3 To PC9 Enable : If high, when the programmable timer 3 times out, it will set PC9 low.	0
15	TMR3EN	Programmable Timer 3 Enable : 0 = The programmable timeout timer is disabled (stopped). 1 = The programmable timeout timer is enabled.	0

4.4.44 Programmable Timeout Timer Source Register 1 | Configuration Index 02CH

BIT	NAME	FUNCTION	DFLT
1:0	VDTMRSEL<1:0>	Video Activitiy Programmable Timeout Timer Select <1:0> : These two bits select which programmable timeout timer will be reset by video activity. Bits <1:0> — Programmable Timeout Timer 0 0 — 0 0 1 — 1 1 0 — 2 1 1 — 3	00
2	Reserved		X
3	VDTMRSELEN	Video Activity Programmable Timeout Timer Enable : When low, video activity will not reset any programmable timer.. When high, one of the 4 programmable timeout timer (selected by VDTMRSEL<1:0>) will be reset.	0
5:4	HDTMRSEL<1:0>	Hard Drive Activitiy Programmable Timeout Timer Select <1:0> : These two bits select which programmable timeout timer will be reset by hard drive activity. Bits <1:0> — Programmable Timeout Timer 0 0 — 0 0 1 — 1 1 0 — 2 1 1 — 3	00
6	Reserved		X
7	HDTMRSELEN	Hard Drive Activity Programmable Timeout Timer Enable : When low, hard drive activity will not reset any programmable timer. When high, one of the 4 programmable timeout timer (selected by HDTMRSEL<1:0>) will be reset.	0
9:8	FDTMRSEL<1:0>	Floppy Drive Activitiy Programmable Timeout Timer Select <1:0> : These two bits select which programmable timeout timer will be reset by floppy drive activity. Bits <1:0> — Programmable Timeout Timer 0 0 — 0 0 1 — 1 1 0 — 2 1 1 — 3	00
10	Reserved		X
11	FDTMRSELEN	Floppy Drive Activity Programmable Timeout Timer Enable : When low, floppy drive activity will not reset any programmable timer. When high, one of the 4 programmable timeout timer (selected by FDTMRSEL<1:0>) will be reset.	0

13:12	KBTMRSEL<1:0>	Keyboard Activitiy Programmable Timeout Timer Select <1:0> : These two bits select which programmable timeout timer will be reset by keybooard activity. Bits <1:0> — Programmable Timeout Timer 0 0 — 0 0 1 — 1 1 0 — 2 1 1 — 3	00
14	Reserved		X
15	KBTMRSELEN	Keyboard Activity Programmable Timeout Timer Enable : When low, keyboard activity will not reset any programmable timer. When high, one of the 4 programmable timeout timer (selected by KBTMRSEL<1:0>) will be reset.	0

4.4.45 Programmable Timeout Timer Source Register 2		Configuration Index 02DH	
BIT	NAME	FUNCTION	DFLT
1:0	SIOTMRSEL<1:0>	Serial Port Activitiy Programmable Timeout Timer Select <1:0> : These two bits select which programmable timeout timer will be reset by serial port activity. Bits <1:0> — Programmable Timeout Timer 0 0 — 0 0 1 — 1 1 0 — 2 1 1 — 3	00
2	Reserved		X
3	SIOTMRSELEN	Serial Port Activity Programmable Timeout Timer Enable : When low, Serial Port activity will not reset any programmable timer. When high, one of the 4 programmable timeout timer(selected by SIOTMRSEL<1:0>) will be reset.	0
5:4	PIOTMRSEL<1:0>	Parallel Port Activitiy Programmable Timeout Timer Select <1:0> : These two bits select which programmable timeout timerwill be reset by parallel port activity. Bits <1:0> — Programmable Timeout Timer 0 0 — 0 0 1 — 1 1 0 — 2 1 1 — 3	00
6	Reserved		X
7	PIOTMRSELEN	Parallel Port Activity Programmable Timeout Timer Enable : When low, Parallel Port activity will not reset any programmable timer. When high, one of the 4 programmable timeout timer (selected by PIOTMRSEL<1:0>) will be reset.	0
9:8	PR0TMRSEL<1:0>	Programmable Range 0 Activitiy Timer Select <1:0> : These two bits select which programmable timeout timer will be reset by programmable range 0 activity. Bits <1:0> — Programmable Timeout Timer 0 0 — 0 0 1 — 1 1 0 — 2 1 1 — 3	00
10	Reserved		X

11	PR0TMRSELEN	Programmable Range 0 Activity Timer Enable : When low, programmable range 0 activity will not reset any programmable timer. When high, one of the 4 programmable timeout timer (selected by PR0TMRSEL<1:0>) will be reset.	0
13:12	PR1TMRSEL<1:0>	Programmable Range 1 Activitiy Timer Select <1:0> : These two bits select which programmable timeout timer will be reset by programmable range 1 activity. Bits <1:0> — Programmable Timeout Timer 0 0 — 0 0 1 — 1 1 0 — 2 1 1 — 3	00
14	Reserved		X
15	PR1TMRSELEN	Programmable Range 1 Activity Timer Enable : When low, programmable range 1 activity will not reset any programmable timer. When high, one of the 4 programmable timeout timer (selected by PR1TMRSEL<1:0>) will be reset.	0

4.4.46 Programmable Timeout Timer Source Register 3		Configuration Index 02EH	
BIT	NAME	FUNCTION	DFLT
1:0	PR2TMRSEL<1:0>	Programmable Range 2 Activitiy Timer Select <1:0> : These two bits select which programmable timeout timer will be reset by programmable range 2 activity. Bits <1:0> — Programmable Timeout Timer 0 0 — 0 0 1 — 1 1 0 — 2 1 1 — 3	00
2	Reserved		X
3	PR2TMRSELEN	Programmable Range 2 Activity Timer Enable : When low, programmable range 2 activity will not reset any programmable timer. When high, one of the 4 programmable timeout timer (selected by PR2TMRSEL<1:0>) will be reset.	0
5:4	PR3TMRSEL<1:0>	Programmable Range 3 Activitiy Timer Select <1:0> : These two bits select which programmable timeout timer will be reset by programmable range 3 activity. Bits <1:0> — Programmable Timeout Timer 0 0 — 0 0 1 — 1 1 0 — 2 1 1 — 3	00
6	Reserved		X
7	PR3TMRSELEN	Programmable Range 3 Activity Timer Enable : When low, programmable range 3 activity will not reset any programmable timer. When high, one of the 4 programmable timeout timer (selected by PR3TMRSEL<1:0>) will be reset.	0
15:8	Reserved		0

4.4.47 Programmable Timeout Timer Source Register 4		Configuration Index 02FH	
BIT	NAME	FUNCTION	DFLT
1:0	EXT0TMRSEL<1:0>	External Activitiy 0 Programmable timeout timer Select <1:0> : These two bits select which programmable timeout timer will be reset by EXTACT0 input Bits <1:0> — Programmable Timeout Timer 0 0 — 0 0 1 — 1 1 0 — 2 1 1 — 3	00
2	Reserved		X
3	EXT0TMRSELEN	External Activity 0 Programmable timeout timer Enable : When low, EXTACT0 input will not reset any programmable timer. When high, one of the 4 programmable timeout timer (selected by EXT0TMRSEL<1:0>) will be reset.	0
5:4	EXT1TMRSEL<1:0>	External Activitiy 1 Programmable timeout timer Select <1:0> : These two bits select which programmable timeout timer will be reset by EXTACT1 input Bits <1:0> — Programmable Timeout Timer 0 0 — 0 0 1 — 1 1 0 — 2 1 1 — 3	00
6	Reserved		X
7	EXT1TMRSELEN	External Activity 1 Programmable timeout timer Enable : When low, EXTACT1 input will not reset any programmable timer. When high, one of the 4 programmable timeout timer (selected by EXT1TMRSEL<1:0>) will be reset.	0
9:8	EXT2TMRSEL<1:0>	External Activitiy 2 Programmable timeout timer Select <1:0> : These two bits select which programmable timeout timer will be reset by EXTACT2 input Bits <1:0> — Programmable Timeout Timer 0 0 — 0 0 1 — 1 1 0 — 2 1 1 — 3	00
10	Reserved		X
11	EXT2TMRSELEN	External Activity 2 Programmable timeout timer Enable : When low, EXTACT2 input will not reset any programmable timer. When high, one of the 4 programmable timeout timer (selected by EXT2TMRSEL<1:0>) will be reset.	0
13:12	EXT3TMRSEL<1:0>	External Activitiy 3 Programmable timeout timer Select <1:0> : These two bits select which programmable timeout timer will be reset by EXTACT3 input Bits <1:0> — Programmable Timeout Timer 0 0 — 0 0 1 — 1 1 0 — 2 1 1 — 3	00
14	Reserved		X

15	EXT3TMRSELEN	External Activity 3 Programmable timeout timer Enable : When low, EXTACT3 input will not reset any programmable timer. When high, one of the 4 programmable timeout timer (selected by EXT3TMRSEL<1:0>) will be reset.	0

4.5 Cache Controller Register Specifications

4.5.0 Cache Control Register 1 — Configuration Index 400H

BIT	NAME	FUNCTION	DFLT
3:0	L2CST<3:0>	Level 2 Cache Status : Bits <3:0> — Level 2 Cache Status 0 0 0 0 — StandBy 0 0 0 1 — Initialization 0 0 1 0 — Write Through 0 0 1 1 — Write Back 0 1 0 0 — Flush 0 1 0 1 — Write Through Data Retention 0 1 1 0 — Write Back Data Retention All others — Reserved	0H
7:4	CSIZE<3:0>	Level 2 Cache Data Size : Bits <2:0> — Level 2 Cache Size 0 0 0 0 — Reserved 0 0 0 1 — 64KB, Two Banks 0 0 1 0 — 128KB, Single Bank 0 0 1 1 — 256KB, Two Banks 0 1 0 0 — 512KB, Single Bank 0 1 0 1 — 1MB, Two Banks 1 0 1 1 — 256KB, Single Bank (Two 64Kx16) All others — Reserved	1H
8	L1WB	Enable Level 1 cache write back support : 0 = Disabled, 1 = Enabled.	0
9	WPL2KEN	L2 Cache Write Protect : 0 = L2 will not cache any write protected region. 1 = Write protected address is also cacheable in L2 cache.	0
15:10	Reserved		XXH

4.5.1 Cache Control Register 2 — Configuration Index 401H

BIT	NAME	FUNCTION	DFLT
0	TWIDTH	Width of L2 cache TAG Data : 0 = 8 bits, 1 = 9 bits	0
1	DTYEN	Configuration of Level 2 Cache TAG Field : 0 = Use all TAG bits as address bits 1 = Use one TAG bit as dirty bit, the rest will be address bits	1
2	DRTWEN	Configuration of Level 2 Cache TAG write control : 0 = Single Write Enable control for both Dirty and TAG Address 1 = Separate Write Enable signals for Dirty and TAG Address	1
3	Reserved		0
4	Reserved		0
6:5	Reserved		01

7	EHITEN	An external comparator is used. 0 = No external comparator, 1 = With external comparator.	0
15:8	Reserved		XXH

4.5.2 Cache Control Register 3 — Configuration Index 402H

BIT	NAME	FUNCTION	DFLT
1:0	RDL<1:0>	CPU cache read lead-off cycles Bits <1:0> — CPU read lead-off cycles 0 0 — 2 T (zero wait states) 0 1 — 3 T (one wait state) 1 0 — 4 T (two wait states) 1 1 — Reserved	10
2	RDB2T	CPU cache read burst cycles 0 = 1 T (zero wait states), 1 = 2 T (one wait state)	1
4:3	WRL<1:0>	CPU cache write lead-off cycles Bits <1:0> — CPU write lead-off cycles 0 0 — 2 T (zero wait states) 0 1 — 3 T (one wait state) 1 0 — 4 T (two wait states) 1 1 — Reserved	10
5	WRB2T	CPU cache write burst cycles 0 = 1 T (zero wait states), 1 = 2 T (one wait state)	1
7:6	Reserved		01
9:8	Reserved		00
15:10	Reserved		XXH

4.5.3 Reserved — Configuration Index 403H

BIT	NAME	FUNCTION	DFLT
0	Reserved		0
2:1	Reserved		11
4:3	Reserved		10
5	Reserved		0
15:6	Reserved		XXH

4.5.4 Reserved — Configuration Index 404H

BIT	NAME	FUNCTION	DFLT
0	Reserved		1
1	Reserved		1
2	Reserved		1
3	Reserved		1
4	Reserved		0
7:5	Reserved		XH
15:8	Reserved		00H

4.6 Global Control Register Specification

This register is write only in REDWOOD1. To read its contents, use index 780H.

4.6.0 Global Control Register 1			Configuration Index 700H
BIT	NAME	FUNCTION	DFLT
0	CPUHITMWS	CPU HITM# sampling wait state selection : 1 = The sampling point for CPU HITM# input will be delayed by 1 T state. 0 = No additional delay.	0
1	Reserved		0
2	Reserved		0
3	Reserved		0
13:	Reserved		000H
14	Reserved		0
15	Reserved		0

5.0 REDWOOD 2 Register Specifications

5.1 Bus Controller Register Specifications

5.1.0 AT Miscellaneous Control Register 1		Configuration Index 300H	
BIT	NAME	FUNCTION	DFLT
2:0	SYSDIV<2:0>	SYSCLK Divisor Selects, 2 to 0: Bits<2:0> Divided By 0H Reserved 1H 3 2H 4 3H 5 4H 6 5H Reserved 6H Reserved 7H Reserved	4H
3	Reserved		X
5:4	ATRDYDLY<1:0>	AT Ready Delay Selects, 1:0: Bits<1:0> AT Ready Delay 0H No Delay 1H 1 HS1XCLK 2H 2 HS1XCLK 3H Reserved	2H
7:6	B2BD<1:0>	Back To Back I/O Delay Selects, 1 to 0: Bits<1:0> I/O Spacing in SYSCLK's 0H 0 1H 1 2H 2 3H 3	3H
8	Reserved		X
9	PARITYEN	Global Parity Enable : This is the global enable bit for the parity circuit. When low, the parity is disabled. When high. the parity is enabled.	0
10	ATREFDIS	AT Bus Refresh Disable: When high, the AT Bus refresh function will be disabled.	0
11	HIDREFEN	Hidden AT Refresh Enable : If high, AT refresh cycle will not hold CPU. If low, it will.	1
15:12	Reserved		XH

5.1.1 AT Miscellaneous Control Register 2			Configuration Index 301H
BIT	NAME	FUNCTION	DFLT
2:0	IDECMDW<2:0>	Turbo IDE Command Width Selects 2:0: Bits<2:0> — Turbo IDE Command Width 0H — 2 HS1XCLK 1H — 3 HS1XCLK 2H — 4 HS1XCLK 3H — 5 HS1XCLK 4H — 6 HS1XCLK 5H — 7 HS1XCLK 6H — 8 HS1XCLK 7H — 9 HS1XCLK	7H
5:3	IDEB2BDLY<2:0>	Turbo IDE Back To Back Cycle Delay Selects 2:0 : Bits<2:0> — Back To Back Cycle Delay 0H — 2 HS1XCLK 1H — 4 HS1XCLK 2H — 6 HS1XCLK 3H — 8 HS1XCLK 4H — 10 HS1XCLK 5H — 12 HS1XCLK 6H — 14 HS1XCLK 7H — 16 HS1XCLK	7H
6	GIDEENABLE	Global IDE Enable : This is the global enable bit for the IDE control function. When low, the IDE function is disabled. When high, the function is enabled.	0
7	Reserved		0
9:8	Reserved		00
10	Reserved		0
11	EXTATADD	Extended AT Address: When High, address bits A<25:24> will be ignored by AT select logic such that AT cycles in the 16-64MB range will propogate to the AT Bus, though they will alias if above the 16MB AT boundry.	0
12	DLYLOCAL	Delay the sampling point for LOCAL#. If low, the sampling point for LOCAL# is the end of first T2. If high, the sampling point will be delayed to the end of second T2.	1
13	Reserved		0
14	BSEREN	BSER Enable : When high, BSER function to REDWOOD2/FIR2 will be enabled. When low, BSER will stay high always and the function will be disabled.	0
15	Reserved		0

5.1.2 REDWOOD 2 Identification Register			Configuration Index 310H
BIT	NAME	FUNCTION	DFLT
3:0	R2ID<3:0>	REDWOOD 2 Revision number ID <3:0> : 0H = Initial Revision. 1H = A-step silicon. These bits are read only.	1H
15:4	Reserved		XXXH

5.2 REDWOOD 2 Pin Function Select Register

5.2.0 REDWOOD 2 Pin Select Register			Configuration Index 302H
BIT	NAME	FUNCTION	DFLT
0	DPBUSEN#	DP BUS ENable # : If low, DP<3:0> are the parity data bits. If high, use index 302H, bits <3:1> below.	0
1	GPIOPINEN#	GPIO<7:4> PIN ENable # : If 302H, bit 0 is high and this bit is low, DP<3:0> pins become GPIO<7:4> and their functions can be controlled by index register 304H, bits <15:8>.	0
2	Reserved		0
3	Reserved		0
4	IDEPINEN	IDE Pin Enable : If low, DRQ7, DRQ6, DRQ5 and DRQ3 are their normal DMA Request Inputs. If high, these pins become IDEBUFEN#, IDED7, IDECS1# and IDECS0# respectively.	0
5	LOCALPINEN	Additional LOCAL Pin Enable : When high, LREQ1# pin becomes LOCAL2# input for additional VL Bus device and LGNT1# pin becomes LOCAL1#. When low, they are LREQ1# and LGNT1# respectively.	0
6	Reserved		0
7	Reserved		0
8	ATREFADDEN	AT Refresh Address Enable : If high, SD<15:8> will become AT refresh address SA<7:0> during AT refresh cycles. Note : An external buffer chip is needed between SD<15:8> and SA<7:0> with AT REFRESH# as the enable signal.	0
9	Reserved		0
10	Reserved		0
11	Reserved		0
12	CPU386EN	CPU 386 Type ENable : If high, then HITM# pin is IRQ13 input from the numeric coprocessor and FERR# pin is W/R# status from the CPU. Should use index register 100H, bit 1 high to determine if this bit should be programmed to high.	0
13	Reserved		0
14	Reserved		0
15		REDWOOD Type Select : If high, the device type is REDWOOD If low, it is FIR. This bit is sampled at SAEN# pin at RESET# leading edge and is otherwise read only.	1

5.3 Miscellaneous Peripheral Control Register Specifications

5.3.0 Miscellaneous DMA Control Register 1			Configuration Index 330H
BIT	NAME	FUNCTION	DFLT
7:0	Reserved		00H
8	ENCDDMA	Encoded DMA Acknowledges : If high, the 7 channel DMA Acknowledge outputs should be encoded into 3 signals. If low, it should follow the regular 7 channels.	0
15:9	Reserved		XXH

5.3.1 Miscellaneous DMA Control Register 2		Configuration Index 331H	
BIT	NAME	FUNCTION	DFLT
0	SEL3DMA	Select 3 DMA channel mode : 0 = All regular 7 DMA channels are used. 1 = DMA channels are limited to 3. Each channel can be programmed to be one of the 7 channels.	0
3:1	Reserved		X
6:4	DMA0CHSEL<2:0>	DMA channel 0 select <2:0> : These bits are used in a 3 DMA channel system environment. Those 3 DMA channles can be routed to any of the 7 DMA channels available in PC-AT system. Following is the table how to route the DMA channel 0 (index 331H bit 0 should be set "1"): Bits <2:0> — DMA channel 0H — 0 1H — 1 2H — 2 3H — 3 4H — Not Used 5H — 5 6H — 6 7H — 7	5H
7	Reserved		X
10:8	DMA1CHSEL<2:0>	DMA channel 1 select <2:0> : Bits <2:0> — DMA channel 0H — 0 1H — 1 2H — 2 3H — 3 4H — Not Used 5H — 5 6H — 6 7H — 7	1H
11	Reserved		X
14:12	DMA2CHSEL<2:0>	DMA channel 2 select <2:0> : Bits <2:0> — DMA channel 0H — 0 1H — 1 2H — 2 3H — 3 4H — Not Used 5H — 5 6H — 6 7H — 7	2H
15	Reserved		X

5.3.2 Reserved		Configuration Index 340H	
BIT	NAME	FUNCTION	DFLT
0	ENBINT	Enable BINT input : 0 = BINT is disabled, 1 = BINT is enabled.	0
1	Reserved		0
15:2	Reserved		

5.3.3 Reserved			Configuration Index 341H
BIT	NAME	FUNCTION	DFLT
0	Reserved		0
1	Reserved		0
2	Reserved		0
3	Reserved		0
4	Reserved		0
5	Reserved		0
6	Reserved		0
7	Reserved		0
8	Reserved		0
9	Reserved		0
10	Reserved		0
11	Reserved		0
12	Reserved		0
13	Reserved		0
14	Reserved		0
15	Reserved		0

5.4 Additional Power Management Register Specifications

5.4.0 Modular Clock Control Register			Configuration Index 303H
BIT	NAME	FUNCTION	DFLT
0	ATMODCLKEN	AT Modular Clock Enable : 0 = AT Modular Clock Function is disabled. 1 = AT Modular Clock Function is enabled.	0
1	Reserved		0
3:2	Reserved		XX
4	TMRCLKDIS	Timer Clock Disable : When high, stops the TMRCLK to the 8254 in the 82C206 module. When low, will not stop the TMRCLK.	0
5	SYSCLKDIS	ISA SYSCLK Disable : When high, stops the SYSCLK to the ISA Bus when the bus is idle. When low, will not stop the SYSCLK.	0
15:6	Reserved		XXH

5.4.1 Primary Activities IRQ Mask Register			Configuration Index 350H
BIT	NAME	FUNCTION	DFLT
7:0	Reserved		XXH
8	PAMSKIRQ8	IRQ 8 Primary Activity Mask Enable Function : When high, IRQ8 will not trigger any primary activity. When low, it will.	1
9	PAMSKIRQ9	IRQ 9 Primary Activity Mask Enable Function : When high, IRQ9 will not trigger any primary activity. When low, it will.	1
10	PAMSKIRQ10	IRQ 10 Primary Activity Mask Enable Function : When high, IRQ10 will not trigger any primary activity. When low, it will.	1
11	PAMSKIRQ11	IRQ 11 Primary Activity Mask Enable Function : When high, IRQ11 will not trigger any primary activity. When low, it will.	1

12	PAMSKIRQ12	IRQ 12 Primary Activity Mask Enable Function : When high, IRQ12 will not trigger any primary activity. When low, it will.	1
13	PAMSKIRQ13	IRQ 13 Primary Activity Mask Enable Function : When high, IRQ13 will not trigger any primary activity. When low, it will.	1
14	PAMSKIRQ14	IRQ 14 Primary Activity Mask Enable Function : When high, IRQ14 will not trigger any primary activity. When low, it will.	1
15	PAMSKIRQ15	IRQ 15 Primary Activity Mask Enable Function : When high, IRQ15 will not trigger any primary activity. When low, it will.	1

5.4.2 PMI Trigger Source IRQ Active Register		Configuration Index 351H	
BIT	NAME	FUNCTION	DFLT
0	PMIDETBACTV	PMI Trigger Source DeTurbo Switch active : When high, it indicates the PMI is triggered by the changing state of DeTurbo Switch. Writing a "0" to this bit will clear it; writing a "1" will have no effect.	0
7:1	Reserved		XXH
8	PMIIRQ8ACTV	PMI Trigger Source IRQ8 active : When high, it indicates the PMI is triggered by IRQ8. Writing a "0" to this bit will clear it; writing a "1" will have no effect. This bit must be cleared after the PMI source bits have been cleared in index register 001H.	0
9	PMIIRQ9ACTV	PMI Trigger Source IRQ9 active : When high, it indicates the PMI is triggered by IRQ9. Writing a "0" to this bit will clear it; writing a "1" will have no effect. This bit must be cleared after the PMI source bits have been cleared in index register 001H.	0
10	PMIIRQ10ACTV	PMI Trigger Source IRQ10 active : When high, it indicates the PMI is triggered by IRQ10. Writing a "0" to this bit will clear it; writing a "1" will have no effect. This bit must be cleared after the PMI source bits have been cleared in index register 001H.	0
11	PMIIRQ11ACTV	PMI Trigger Source IRQ11 active : When high, it indicates the PMI is triggered by IRQ11. Writing a "0" to this bit will clear it; writing a "1" will have no effect. This bit must be cleared after the PMI source bits have been cleared in index register 001H.	0
12	PMIIRQ12ACTV	PMI Trigger Source IRQ12 active : When high, it indicates the PMI is triggered by IRQ12. Writing a "0" to this bit will clear it; writing a "1" will have no effect. This bit must be cleared after the PMI source bits have been cleared in index register 001H.	0
13	PMIIRQ13ACTV	PMI Trigger Source IRQ13 active : When high, it indicates the PMI is triggered by IRQ13. Writing a "0" to this bit will clear it; writing a "1" will have no effect. This bit must be cleared after the PMI source bits have been cleared in index register 001H.	0
14	PMIIRQ14ACTV	PMI Trigger Source IRQ14 active : When high, it indicates the PMI is triggered by IRQ14. Writing a "0" to this bit will clear it; writing a "1" will have no effect. This bit must be cleared after the PMI source bits have been cleared in index register 001H.	0
15	PMIIRQ15ACTV	PMI Trigger Source IRQ15 active : When high, it indicates the PMI is triggered by IRQ15. Writing a "0" to this bit will clear it; writing a "1" will have no effect. This bit must be cleared after the PMI source bits have been cleared in index register 001H.	0

5.4.3 PMI Trigger Source IRQ Mask Register		Configuration Index 352H	
BIT	NAME	FUNCTION	DFLT
0	IMSKDETURBO	DeTurbo Switch Triggering PMI Mask Enable Function : When high, Any change state of Deturbo Switch will not trigger PMI. When low, mask is disabled, it will trigger PMI.	1
7:1	Reserved		XXH
8	IMSKIRQ8	IRQ 8 Triggering PMI Mask Enable Function : When high, IRQ8 will not trigger PMI. When low, mask is disabled, any IRQ8 will trigger PMI.	1
9	IMSKIRQ9	IRQ 9 Triggering PMI Mask Enable Function : When high, IRQ9 will not trigger PMI. When low, mask is disabled, any IRQ9 will trigger PMI.	1
10	IMSKIRQ10	IRQ 10 Triggering PMI Mask Enable Function : When high, IRQ10 will not trigger PMI. When low, mask is disabled, any IRQ10 will trigger PMI.	1
11	IMSKIRQ11	IRQ 11 Triggering PMI Mask Enable Function : When high, IRQ11 will not trigger PMI. When low, mask is disabled, any IRQ11 will trigger PMI.	1
12	IMSKIRQ12	IRQ 12 Triggering PMI Mask Enable Function : When high, IRQ12 will not trigger PMI. When low, mask is disabled, any IRQ12 will trigger PMI.	1
13	IMSKIRQ13	IRQ 13 Triggering PMI Mask Enable Function : When high, IRQ13 will not trigger PMI. When low, mask is disabled, any IRQ13 will trigger PMI.	1
14	IMSKIRQ14	IRQ 14 Triggering PMI Mask Enable Function : When high, IRQ14 will not trigger PMI. When low, mask is disabled, any IRQ14 will trigger PMI.	1
15	IMSKIRQ15	IRQ 15 Triggering PMI Mask Enable Function : When high, IRQ15 will not trigger PMI. When low, mask is disabled, any IRQ15 will trigger PMI.	1

5.4.4 IRQ Secondary Activity Enable Register		Configuration Index 353H	
BIT	NAME	FUNCTION	DFLT
0	SAMSKIRQ	Secondary Activity Mask for IRQ's : When high, any IRQ will not trigger Secondary Activity.	1
7:1	Reserved		XXH
15:8	Reserved		XXH

5.4.5 Optional GPIO Control Register			Configuration Index 304H
BIT	NAME	FUNCTION	DFLT
7:0	Reserved		XXH
11:8	GPIODATA<7:4>	General Purpose I/O Data 7 to 4: When each bit's corresponding GPIODIR is low, a read of the bit returns the state of the GPIO pin, and a write has no effect. When GPIODIR is high, a read returns the value last written and a write sets the GPIO output to the value written.	0H
15:12	GPIODIR<7:4>	General Purpose I/O Direction 7 to 4: When low GPIO is an input pin. When high GPIO is an output pin.	0H

5.5 Shadow Register Specifications

The following set of Shadow Registers is implemented to provide readability for several system registers that are normally implemented as write only. These shadow registers are read through the REDWOOD's configuration register port in order to avoid potential contention at the original address.

5.5.0 8254 Counter 0 Shadow Register 1			Configuration Index 500H
BIT	BYTE ADD	REGISTER DESCRIPTION	DFLT
7:0	40H	8254 Counter 0 initial count low byte	00H
15:8	Reserved		XXH

5.5.1 8254 Counter 0 Shadow Register 2			Configuration Index 501H
BIT	BYTE ADD	REGISTER DESCRIPTION	DFLT
7:0	40H	8254 Counter 0 initial count high byte	00H
15:8	Reserved		XXH

5.5.2 8254 Counter 1 Shadow Register 1			Configuration Index 502H
BIT	BYTE ADD	REGISTER DESCRIPTION	DFLT
7:0	41H	8254 Counter 1 initial count low byte	00H
15:8	Reserved		XXH

5.5.3 8254 Counter 1 Shadow Register 2			Configuration Index 503H
BIT	BYTE ADD	REGISTER DESCRIPTION	DFLT
7:0	41H	8254 Counter 1 initial count high byte	00H
15:8	Reserved		XXH

5.5.4 8254 Counter 2 Shadow Register 1			Configuration Index 504H
BIT	BYTE ADD	REGISTER DESCRIPTION	DFLT
7:0	42H	8254 Counter 2 initial count low byte	00H
15:8	Reserved		XXH

5.5.5 8254 Counter 2 Shadow Register 2			Configuration Index 505H
BIT	BYTE ADD	REGISTER DESCRIPTION	DFLT
7:0	42H	8254 Counter 2 initial count high byte	00H
15:8	Reserved		XXH

5.5.6 8254 Counter 0 Shadow Register 3			Configuration Index 506H
BIT	BYTE ADD	REGISTER DESCRIPTION	DFLT
7:0	43H	8254 Counter 0 Control Word	00H
15:8	Reserved		00H

5.5.7 8254 Counter 1 Shadow Register 3			Configuration Index 507H
BIT	BYTE ADD	REGISTER DESCRIPTION	DFLT
7:0	43H	8254 Counter 1 Control Word	00H
15:8	Reserved		00H

5.5.8 8254 Counter 2 Shadow Register 3			Configuration Index 508H
BIT	BYTE ADD	REGISTER DESCRIPTION	DFLT
7:0	43H	8254 Counter 2 Control Word	00H
15:8	Reserved		00H

5.5.9 8237 DMA Controller Shadow Register 1			Configuration Index 510H
BIT	BYTE ADD	REGISTER DESCRIPTION	DFLT
7:0	0BH	8237 DMA Controller mode register for channel 0	00H
15:8	Reserved		00H

5.5.10 8237 DMA Controller Shadow Register 2			Configuration Index 511H
BIT	BYTE ADD	REGISTER DESCRIPTION	DFLT
7:0	0BH	8237 DMA Controller mode register for channel 1	00H
15:8	Reserved		00H

5.5.11 8237 DMA Controller Shadow Register 3		Configuration Index 512H	
BIT	BYTE ADD	REGISTER DESCRIPTION	DFLT
7:0	0BH	8237 DMA Controller mode register for channel 2	00H
15:8	Reserved		00H

5.5.12 8237 DMA Controller Shadow Register 4		Configuration Index 513H	
BIT	BYTE ADD	REGISTER DESCRIPTION	DFLT
7:0	0BH	8237 DMA Controller mode register for channel 3	00H
15:8	Reserved		00H

5.5.13 8237 DMA Controller Shadow Register 5		Configuration Index 514H	
BIT	BYTE ADD	REGISTER DESCRIPTION	DFLT
7:0	0BH	8237 DMA Controller mode register for channel 4	00H
15:8	Reserved		00H

5.5.14 8237 DMA Controller Shadow Register 6		Configuration Index 515H	
BIT	BYTE ADD	REGISTER DESCRIPTION	DFLT
7:0	0D6H	8237 DMA Controller mode register for channel 5	00H
15:8	Reserved		00H

5.5.15 8237 DMA Controller Shadow Register 7		Configuration Index 516H	
BIT	BYTE ADD	REGISTER DESCRIPTION	DFLT
7:0	0D6H	8237 DMA Controller mode register for channel 6	00H
15:8	Reserved		00H

5.5.16 8237 DMA Controller Shadow Register 8		Configuration Index 517H	
BIT	BYTE ADD	REGISTER DESCRIPTION	DFLT
7:0	0D6H	8237 DMA Controller mode register for channel 7	00H
15:8	Reserved		00H

5.5.17 8259 Interrupt Controller Shadow Register 1		Configuration Index 520H	
BIT	BYTE ADD	REGISTER DESCRIPTION	DFLT
7:0	020H	8259 PIC 1 ICW1	00H
15:8	Reserved		00H

5.5.18 8259 Interrupt Controller Shadow Register 2		Configuration Index 521H	
BIT	BYTE ADD	REGISTER DESCRIPTION	DFLT
7:0	021H	8259 PIC 1 ICW2	00H
15:8	Reserved		00H

5.5.19 8259 Interrupt Controller Shadow Register 3		Configuration Index 522H	
BIT	BYTE ADD	REGISTER DESCRIPTION	DFLT
7:0	021H	8259 PIC 1 ICW3	00H
15:8	Reserved		00H

5.5.20 8259 Interrupt Controller Shadow Register 4		Configuration Index 523H	
BIT	BYTE ADD	REGISTER DESCRIPTION	DFLT
7:0	021H	8259 PIC 1 ICW4	00H
15:8	Reserved		00H

5.5.21 8259 Interrupt Controller Shadow Register 5		Configuration Index 524H	
BIT	BYTE ADD	REGISTER DESCRIPTION	DFLT
7:0	020H	8259 PIC 1 OCW2	00H
15:8	Reserved		00H

5.5.22 8259 Interrupt Controller Shadow Register 6		Configuration Index 525H	
BIT	BYTE ADD	REGISTER DESCRIPTION	DFLT
7:0	020H	8259 PIC 1 OCW3	00H
15:8	Reserved		00H

5.5.23 8259 Interrupt Controller Shadow Register 7		Configuration Index 526H	
BIT	BYTE ADD	REGISTER DESCRIPTION	DFLT
7:0	0A0H	8259 PIC 2 ICW1	00H
15:8	Reserved		00H

5.5.24 8259 Interrupt Controller Shadow Register 8		Configuration Index 527H	
BIT	BYTE ADD	REGISTER DESCRIPTION	DFLT
7:0	0A1H	8259 PIC 2 ICW2	00H
15:8	Reserved		00H

5.5.25 8259 Interrupt Controller Shadow Register 9		Configuration Index 528H	
BIT	BYTE ADD	REGISTER DESCRIPTION	DFLT
7:0	0A1H	8259 PIC 2 ICW3	00H
15:8	Reserved		00H

5.5.26 8259 Interrupt Controller Shadow Register 10		Configuration Index 529H	
BIT	BYTE ADD	REGISTER DESCRIPTION	DFLT
7:0	0A1H	8259 PIC 2 ICW4	00H
15:8	Reserved		00H

5.5.27 8259 Interrupt Controller Shadow Register 11		Configuration Index 52AH	
BIT	BYTE ADD	REGISTER DESCRIPTION	DFLT
7:0	0A0H	8259 PIC 2 OCW2	00H
15:8	Reserved		00H

5.5.28 8259 Interrupt Controller Shadow Register 12		Configuration Index 52BH	
BIT	BYTE ADD	REGISTER DESCRIPTION	DFLT
7:0	0A0H	8259 PIC 2 OCW3	00H
15:8	Reserved		00H

5.6 Global Control Register Specification

5.6.0 Global Control Register 1			Configuration Index 700H
BIT	NAME	FUNCTION	DFLT
0	CPUHITMWS	CPU HITM# sampling wait state selection : 1 = The sampling point for CPU HITM# input will be delayed by 1 T state. 0 = No additional delay.	0
1	Reserved		0
2	Reserved		0
3	Reserved		0
13:	Reserved		000H
14	Reserved		0
15	Reserved		0

IBM-AT Standard Register Specification

These registers are IBM AT standard registers. They are accessed through normal addresses without any indexing.

0.1 Register 1 (PortB)			Access Address 061H
BIT	NAME	FUNCTION	DFLT
0	TMR2EN	Timer 2 Enable : When high, Timer 2 in the 8254 will be enabled by making the GATE input high. When low, it will be disabled. This bit is Read/Write-able.	0
1	SPKREN	Speaker Enable : When high, the output of Timer 2 will be gated onto the SPKR output pin. When low, the SPKR pin will be inactive. This bit is Read/Write-able.	0
2	PARDIS	Parity Disable : When high, parity checking is disabled and inhibited from generating NMIs. When low, it is enabled. This bit is Read/Write-able.	0
3	IOCHKDIS	I/O Channel Check Disable : When high, ISA signal IOCHCK# sampling is disabled and inhibited from generating NMIs. When low, it is enabled. This bit is Read/Write-able.	0
4	REFRTGL	Refresh Toggle : This bit toggles on each AT refresh cycle. This bit is read only. Writing to this bit has no effect.	X
5	TMR2OUT	Timer 2 Output : Reading this bit returns the status of the Timer 2 output. This bit is read only. Writing to this bit has no effect.	X
6	IOCKERR	IO Channel Check Error : When high, this bit indicates that an IOCHCK# error has occured. When low, no error has occured. This bit is read only. Writing to this bit has no effect.	X
7	PARERR	Parity Error : When high, this bit indicates that a parity error has occured. When low, no error has occured. This bit is read only. Writing to this bit has no effect.	X

0.2 Register 2 (Port 70H)			Access Address 070H
BIT	NAME	FUNCTION	DFLT
6:0	RTCINDX	Real Timer Clock Index : Writing these bits selects an index value within the RTC CMOS RAM. These 7 bits are used to access up to 128 bytes of RAM. These bits are write only and cannot be read at this standard address. A shadow register is provided through Configuration Register at index 086H.	X
7	NMIDIS	NMI Mask : When high, the NMI output pin will be disabled and no NMIs will be generated. When low, the NMI output will be enabled.	X

0.3 Register 3 (Port 92H)			Access Address 092H
BIT	NAME	FUNCTION	DFLT
0	FSTRST	Alternate Fast CPU Reset : A low to high transition of this bit will trigger a CPU reset 6.7us later. Once set high the bit will remain high until written low but will not re-trigger the reset. This bit parallels an equivalent function in the keyboard controller, but the keyboard controller function is much slower. This bit is Read/Write-able.	0
1	FGATEA20	Fast GATEA20 : When high, this bit has no effect on A20. When low, A20 will effectively be forced low regardless of the state of the A20 driver, This includes assertion of the A20M# signal to a 486 CPU. This bit is Read/Write-able.	0
2	Reserved		0
3	SCLOCK1	Security Lock No. 1 : When this bit is set high, RTC/CMOS RAM index 38H-3FH can not be read nor written. Once this bit is set high, it can only be cleared by power on reset.	0
4	Reserved		0
5	Reserved		0
6	Reserved		0
7	Reserved		0

6.0 AC Timing Characteristics

NOTE: All figures are in nanoseconds.

Symbol	Description	Min	Max
T1	COE# active delay from clock rising		8.5
T2	CCS# delay from ADS#		13.5
T3	CA2/3 delay from ADS#		14.2
T4	CA2/3 delay from clock rising		3.0
T5	BRDY# delay from TAGD		15.9
T6a	CWE# rising from clock falling		5.5
T6b	CWE# rising from clock rising		2.9
T7	CWE# falling from clock rising (replacement)		11.3
T8	COE# rising delay		7.1
T9	COE0/1# avoid time		1.5
T10	TAGWE# (read) falling delay from clock rising		10.8
T11	TAGWE# active to TAGD driving		2.3
T12	TAGWE# (read) rising delay from clock rising		10.8
T13	DRTWE# (read) falling delay from clock rising		13.4
T14	DRTWE# (write) rising delay from clock rising		2.8
T15	DRTWE# active to DIRTY driving	0	0
T16	DRTWE# rising delay from clock rising		0.4
T17	SRMCE# delay from ADS#		10.8
T18	SRMCE# rising delay from clock rising		11.2
T19	TGCS# rising delay from clock rising		8.5
T20	TGCS# falling delay from RDY#		8.5
T21	RAS# rising from clock rising		9.0
T22	RAS# falling from clock rising		6.3
T23	MA from clock falling		12.8
T24	CASA# fallling delay from clock rising		5.0
T25	CASA# rising delay from clock rising		8.3
T25a	BRDY# falling delay from clock rising		11.0
T25b	BRDY# delay from clock rising		13.5
T28	MDEN# rising from clock rising		9.4
T29	MDEN# falling from clock rising		8.8
T29a	MAA delay from clock rising		10.0
T29b	MAB delay from clock rising		10.0
T30	CASB# delay from clock rising		6.1
T30a	CASA# delay from clock rising		5.7
T31	RAS# falling from CASB#		1T

Symbol	Description	Min	Max
T32	CASA# from clock		11.5
T33	CASB# from clock		10.6
T34	RAS# falling from clock		8.0
T35	MDEN# falling from clock		8.8
T44a	CAS# falling from clock rising		5.0
T45	BALE inactive to clock rising		6.0
T46	ZWS# valid setup time to clock falling	14.0	
T47	MEMR# active to clock rising		9.7
T48	Command active hold from IOCHRDY active	161.0	
T49	MEMR# inactive to clock falling		6.0
T50	Zero wait state 16-bit command valid to invalid	118.0	
T51	ZWS# valid hold time to clock falling	16.0	
T52	ZWS# valid from command valid		41.0
T53	IOCHRDY inactive from active command (8-bit)		362.0
T54	SBHE# active to clock rising		68.0
T55	IOW# active to clock rising		67.5
T56	8-bit memory write & 8/16-bit I/O write data setup time	90.0	
T57	IOW# inactive to clock rising		7.0
T58	SD hold time to IOW#	57.0	76.0
T59	SA0 valid to clock rising		64.0
T60	SA1 valid to clock rising		64.0
T61	SD read data setup time	32.0	
T62	16-bit command off time	123.0	
T62a	8-bit command off time	181.0	
T63	SYSCLK rising to CPUCLK rising		15.5
T64	LA[23:17] valid to BALE falling	200.0	
T65	8-bit memory I/O command active to inactive	540.0	
T66	IOR# active to clock rising		69.0
T67	BALE falling to 16-bit I/O or 8-bit command		62.0
T68	16-bit I/O command active to inactive	180.0	
T69	IOR# inactive to clock rising		12.0
T70	IOCS16# active to BALE rising		167.0
T71	SYSCLK period	120.0	
T72	LA[23:17] valid setup time to memory command active	204.0	
T73	BALE active to inactive	65.0	96.0
T74	BALE active to inactive	65.0	96.0

Symbol	Description	Min	Max
T75	16-bit memory command active to inactive	238.0	
T76	MEM16# active to BALE rising		76.0
T77	Read data valid hold from inactive command	0	
T78	SA valid hold from command inactive	46.0	
T79	SBHE# valid to BALE falling	59.0	
T80	SA address valid to BALE falling	94.0	
T81	MEMW# active to clock rising		67.0
T82	16-bit memory write data setup time	30.0	
T83	MEMW# inactive to clock rising		41.0
T84	BALE falling to 16-bit memory command: Type 4		
T85	16-bit memory command active to inactive	238.0	
T86	Write data valid hold from inactive command	54.0	
T87	SAEN# inactive to clock falling		63.0
T88	SAEN# active to clock rising		4.0
T89	A[7:0] hold time to MEMR#	87.0	
T90	A[7:0] setup time to MEMR#	79.0	
T91	MEMREF# setup to MEMR#	120.0	
T92	MEMR#/SMEMR# active pulse width	239.0	
T93	IOCHRDY low from MEMR#	78.0	
T94	REFRESH# active to clock rising		9.0
T95	MEMREF# active to MEMR# inactive	60.0	
T96	REFRESH# inactive to clock rising		75.0
T97	MEMREF# setup to MEMR#	120.0	
T98	MEMR# inactive from IOCHRDY		162.0
T99	SBHE# active to clock rising		
T100	Non-hidden refresh MEMREF# setup to MEMR#	210.0	
T101	MEMR#/SMEMR# active pulsewidth	239.0	
T102	SBHE# active to clock rising		11.0
T103	REFRESH# falling delay from clock rising		8.5
T104	MEMR# falling delay from clock rising		8.0
T105	REFRESH# falling to MEMR# falling: 1 SYSCLK		
T106	REFRESH# falling to REFRESH# rising: 3.5 SYSCLK		
T107	REFRESH# rising delay from clock falling		2.0
T108	Min setup time to MEMR#	83	
T109	MEMR# falling to MEMR# rising: 2.0 SYSCLK		
T110	Min hold time from MEMR#	90.0	
T111	BD to clock rising		6.0
T112	Clock rising delay to BAD# rising		8.9
T113	BDEVI# to clock rising		3.0

Symbol	Description	Min	Max
T114	Clock rising to BD		11.9
T115	Clock rising to BADS# falling		10.6
T116	CMD to IOCHRDY		40.6
T118	BADS# falling to clock rising		6.0
T119	BD to clock rising		6.0
T120	Clock rising to BADS# falling		10.6
T121	Clock rising to BD		15.5
T122	Clock rising to BADS# rising		8.9
T123	Clock rising to RDY#		9.4
T124	Clock rising to BD		12.7
T125	BDEV# falling to clock rising		3.0
T126	Clock falling to IOCHRY rising		15.6
T127	TURBO rising delay from clock rising		10.0
T128	IDECS0#/IDECS1# falling delay from clock rising		11.0
T129	IOR#/IOW# falling delay from clock rising		20.0
T130	IOR#/IOW# rising delay from clock rising		18.0
T131	RDY# falling from clock rising		9.5
T132	IDEBUFER# falling delay from clock rising		14.0
T133	IDECS0#/IDECS1# rising from clock rising		12.0
T134	TURBO falling delay from clock rising		10.5
T135	IDEBUFER# rising from clock rising		15.0

7.0 AC Timing Diagrams

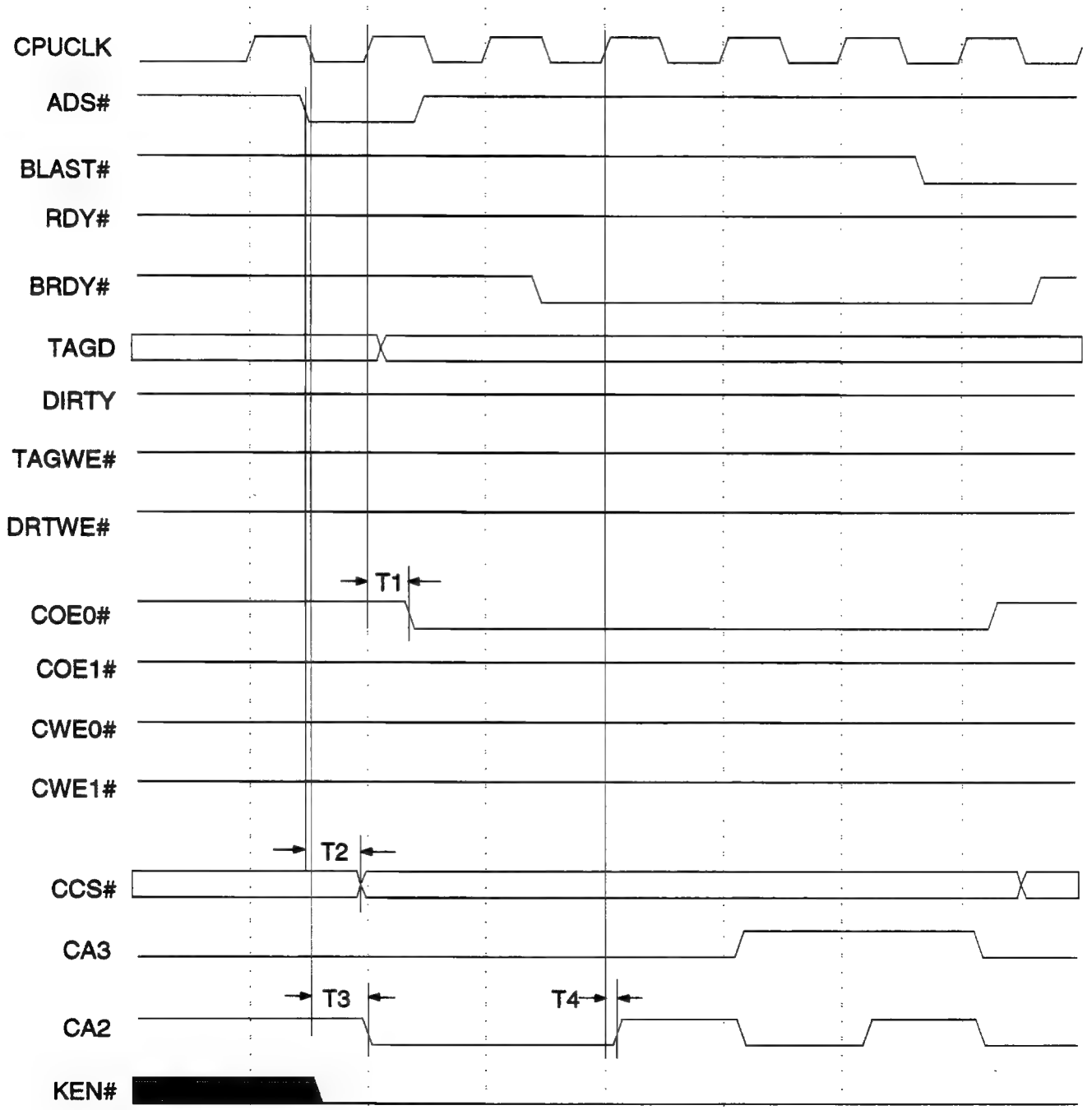
NOTE: In all timing diagrams, capacitance loading is measured at 25pf load.

7.1 Processor Interface

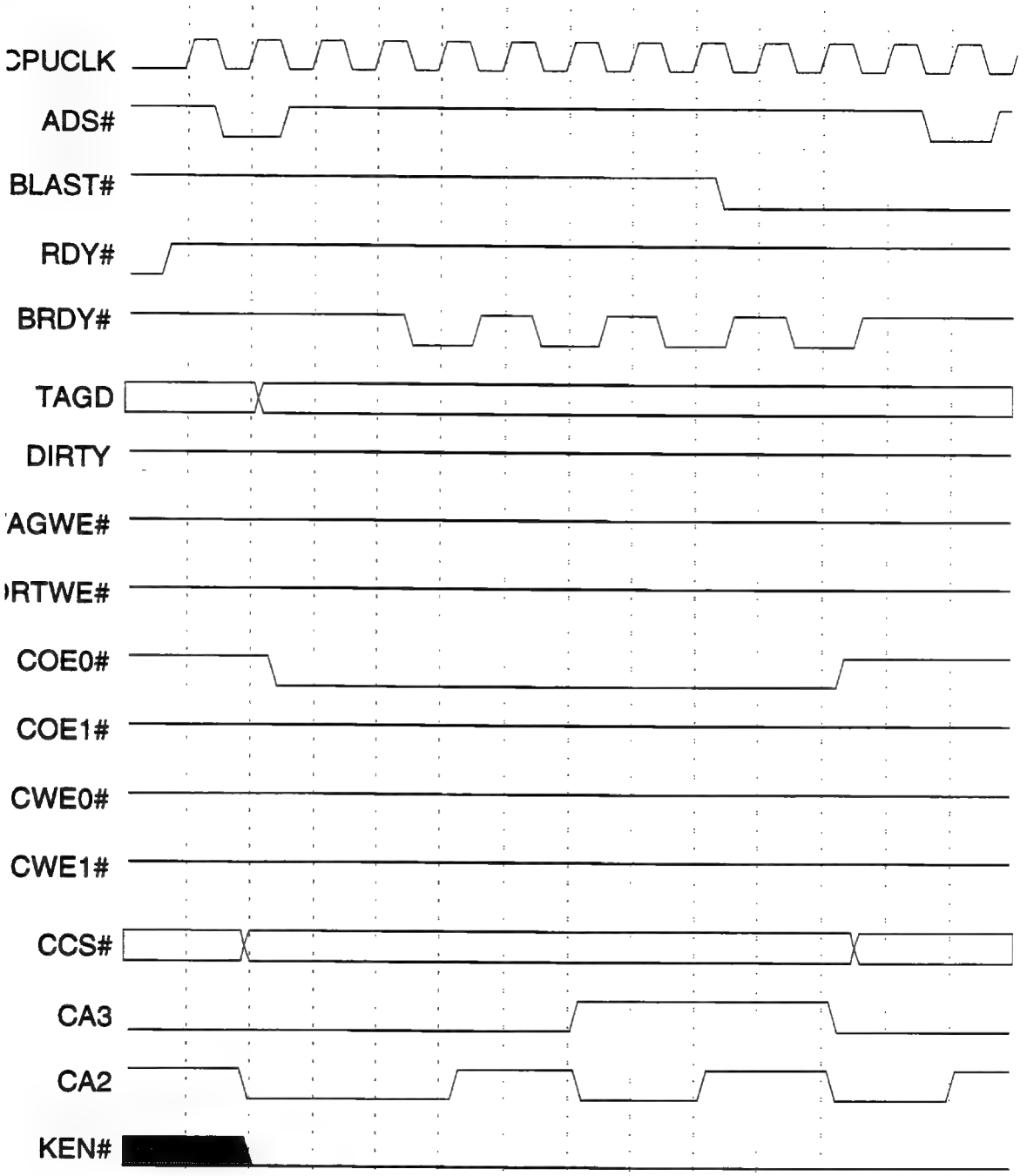
TBD

7.2 Cache Interface

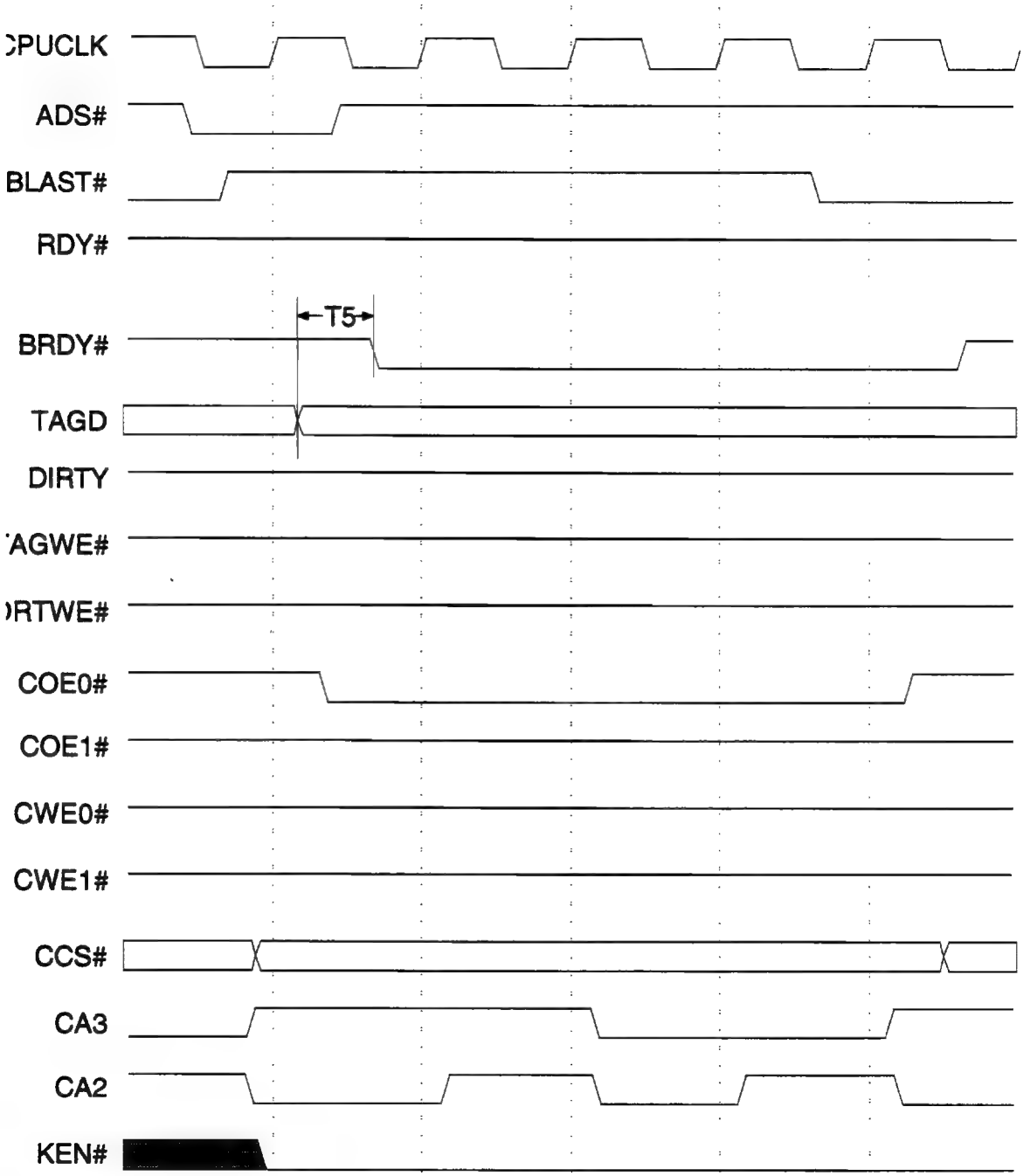
7.2.1 L2 Cache Read Hit *single bank 3-1-1-1 cycle*



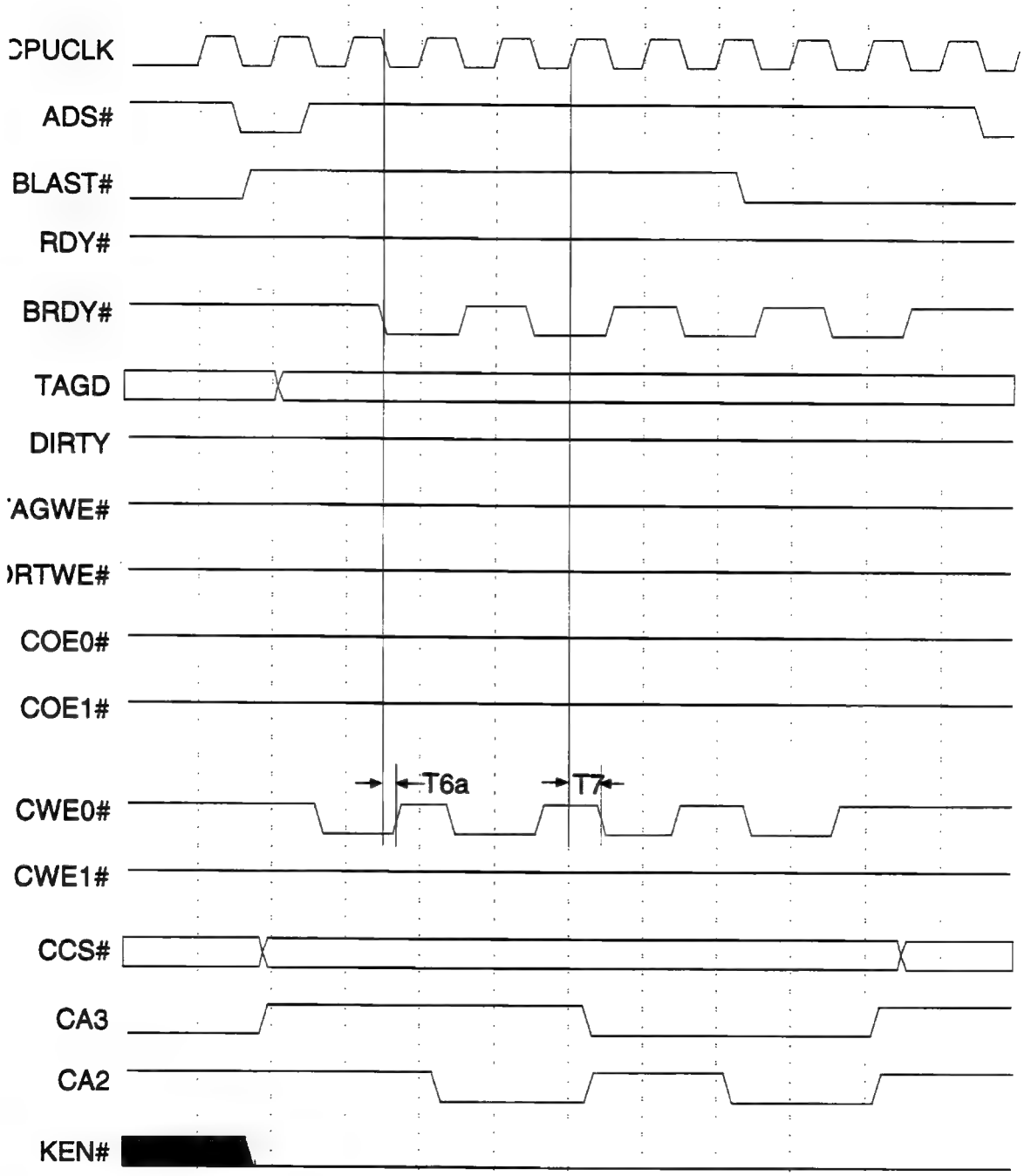
7.2.2 L2 Cache Read Hit single bank 4-2-2-2 cycle



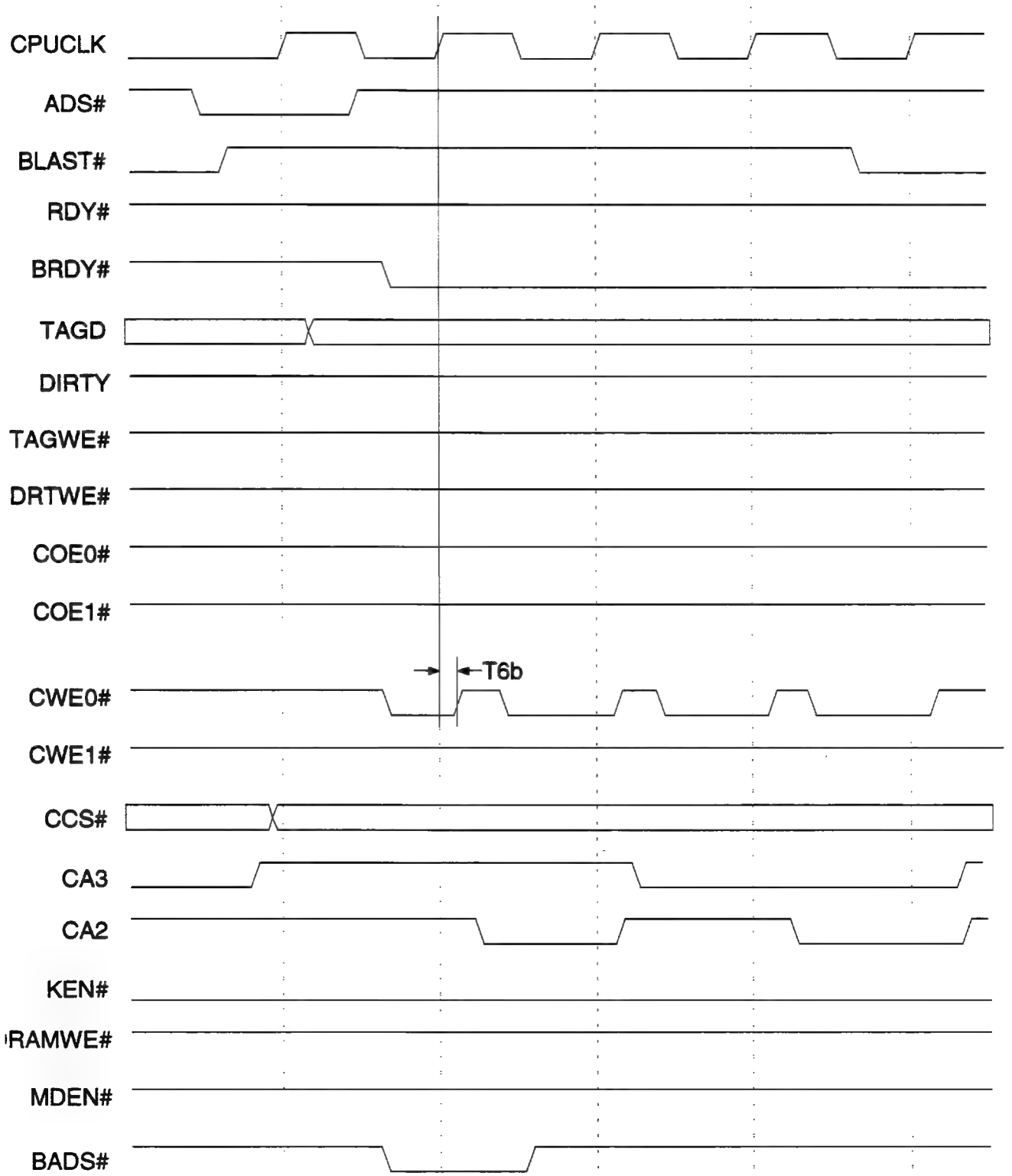
7.2.3 L2 Cache Read Hit single bank 2-1-1-1 cycle



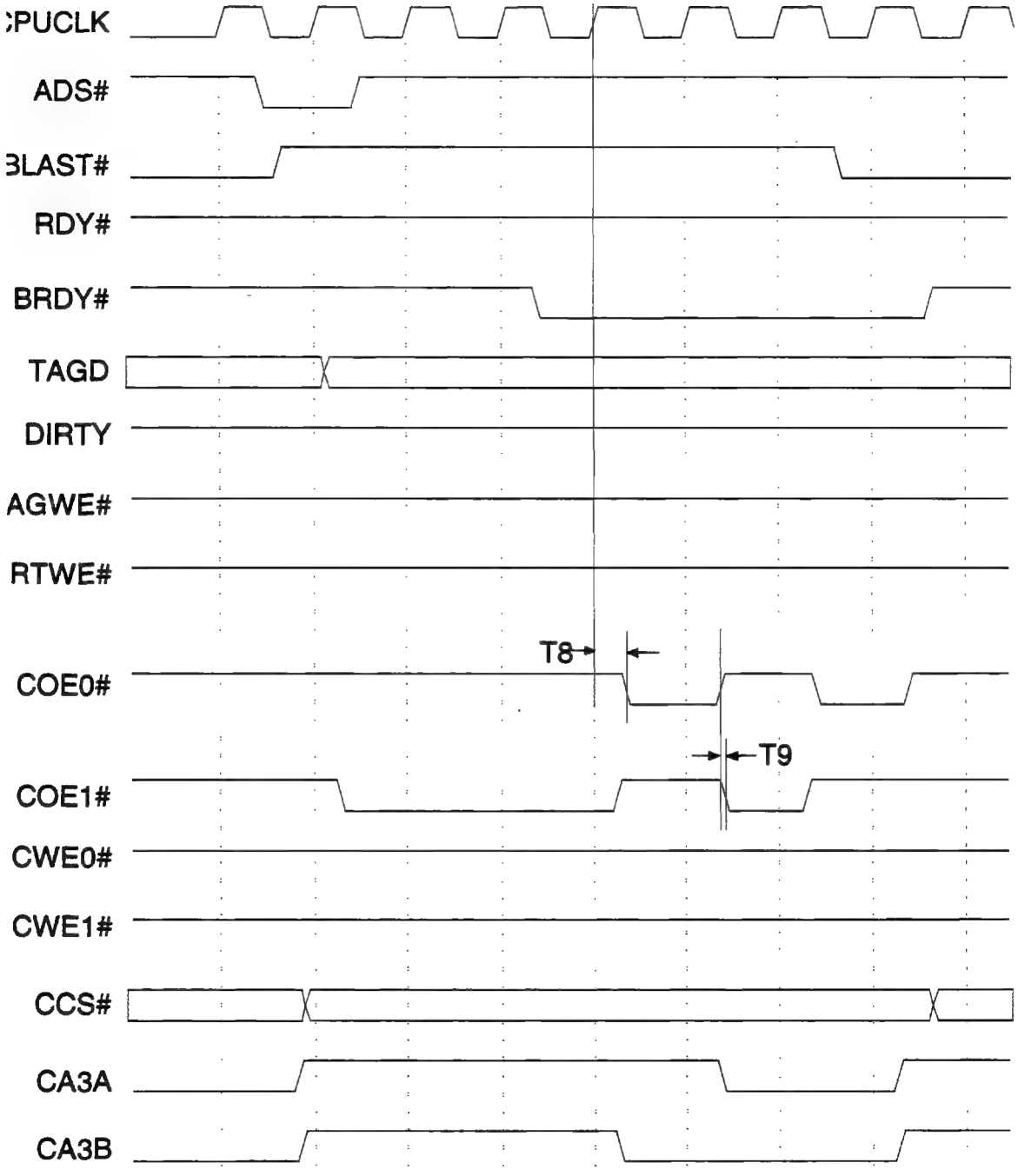
7.2.4 L2 Cache Write Hit 3-2-2-2 cycle write back mode



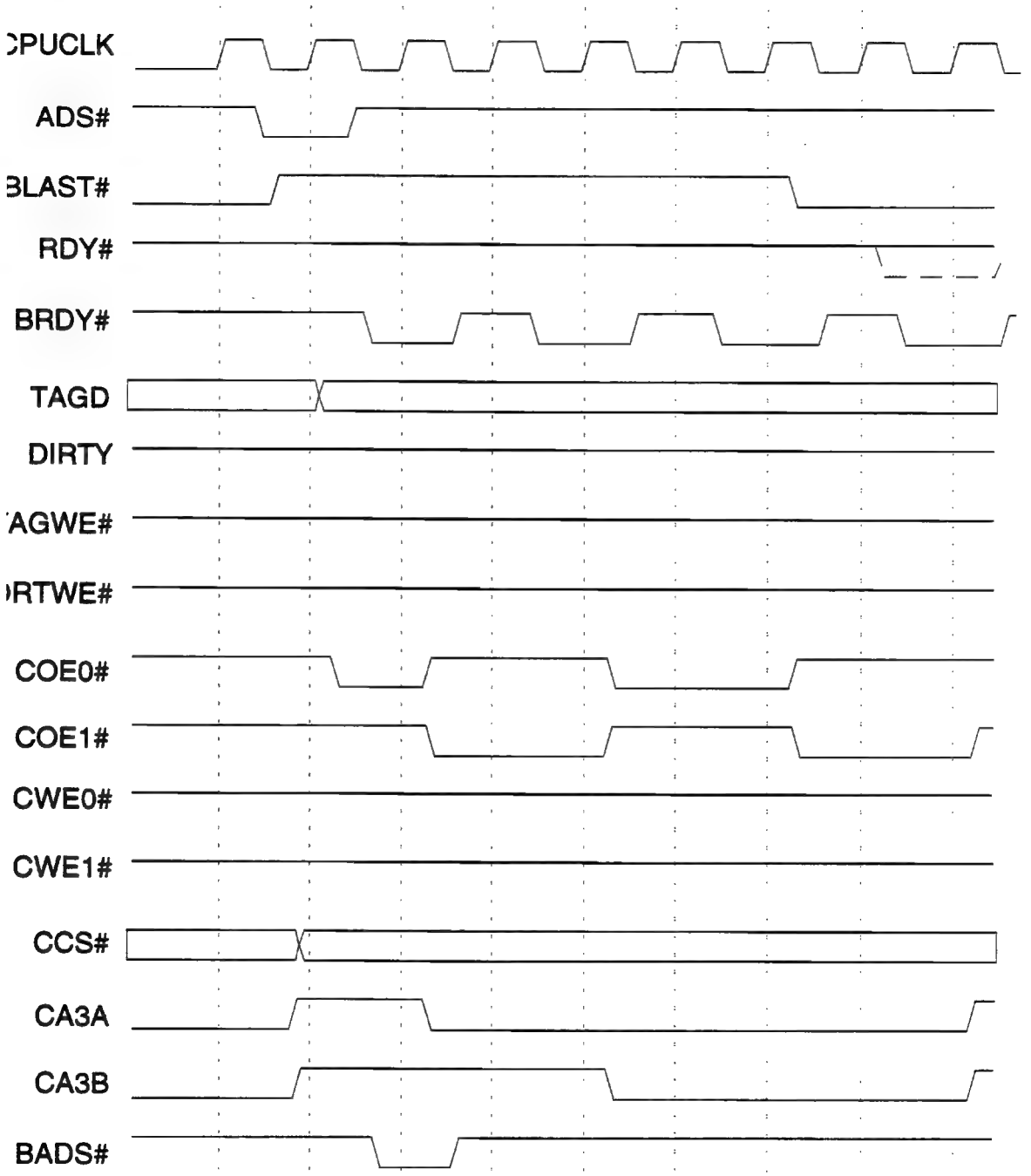
7.2.5 L2 Cache Write Hit single bank 2-1-1-1 cycle write back mode



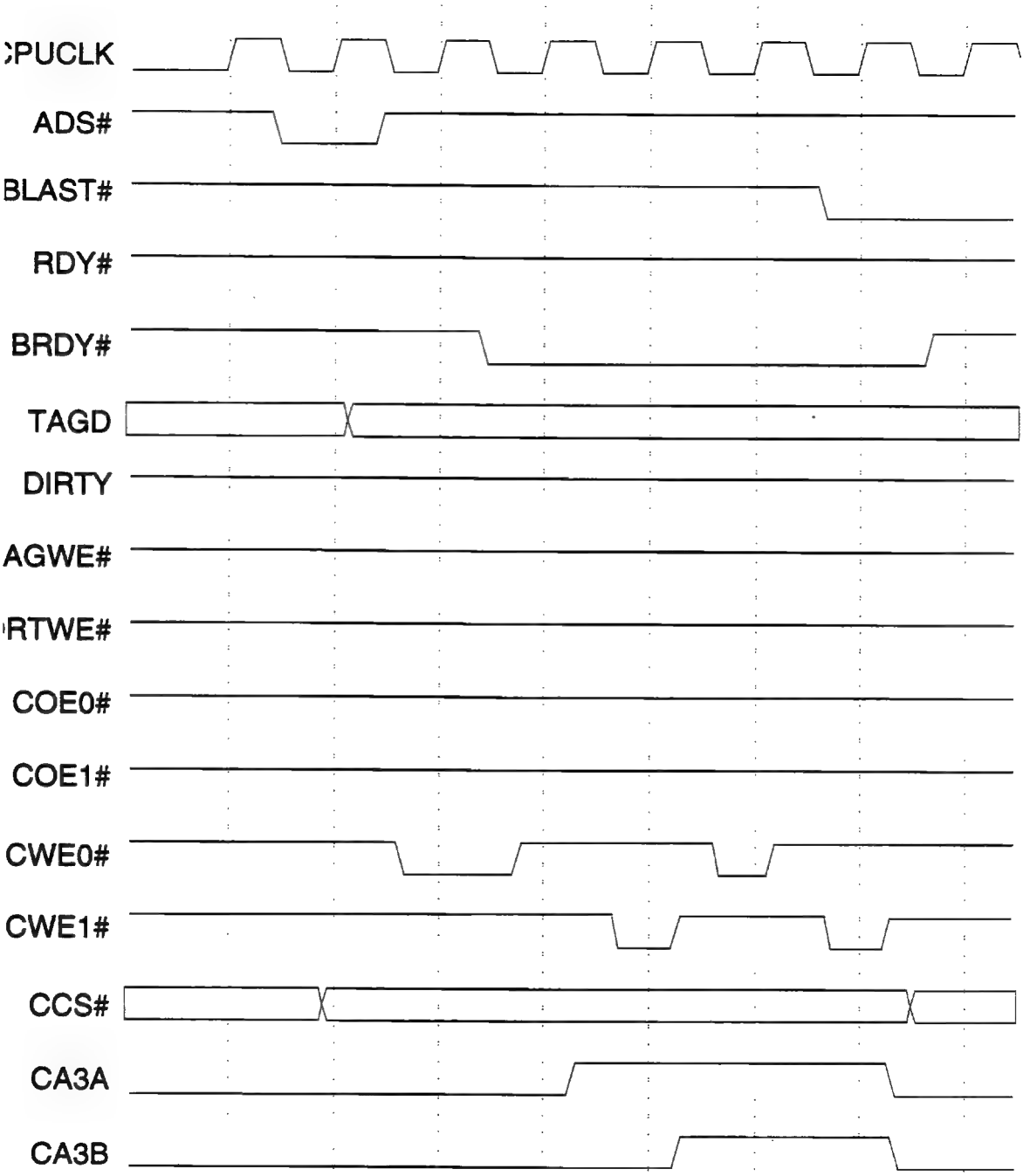
7.2.6 L2 Cache Read Hit dual bank interleave 4-1-1-1 cycle



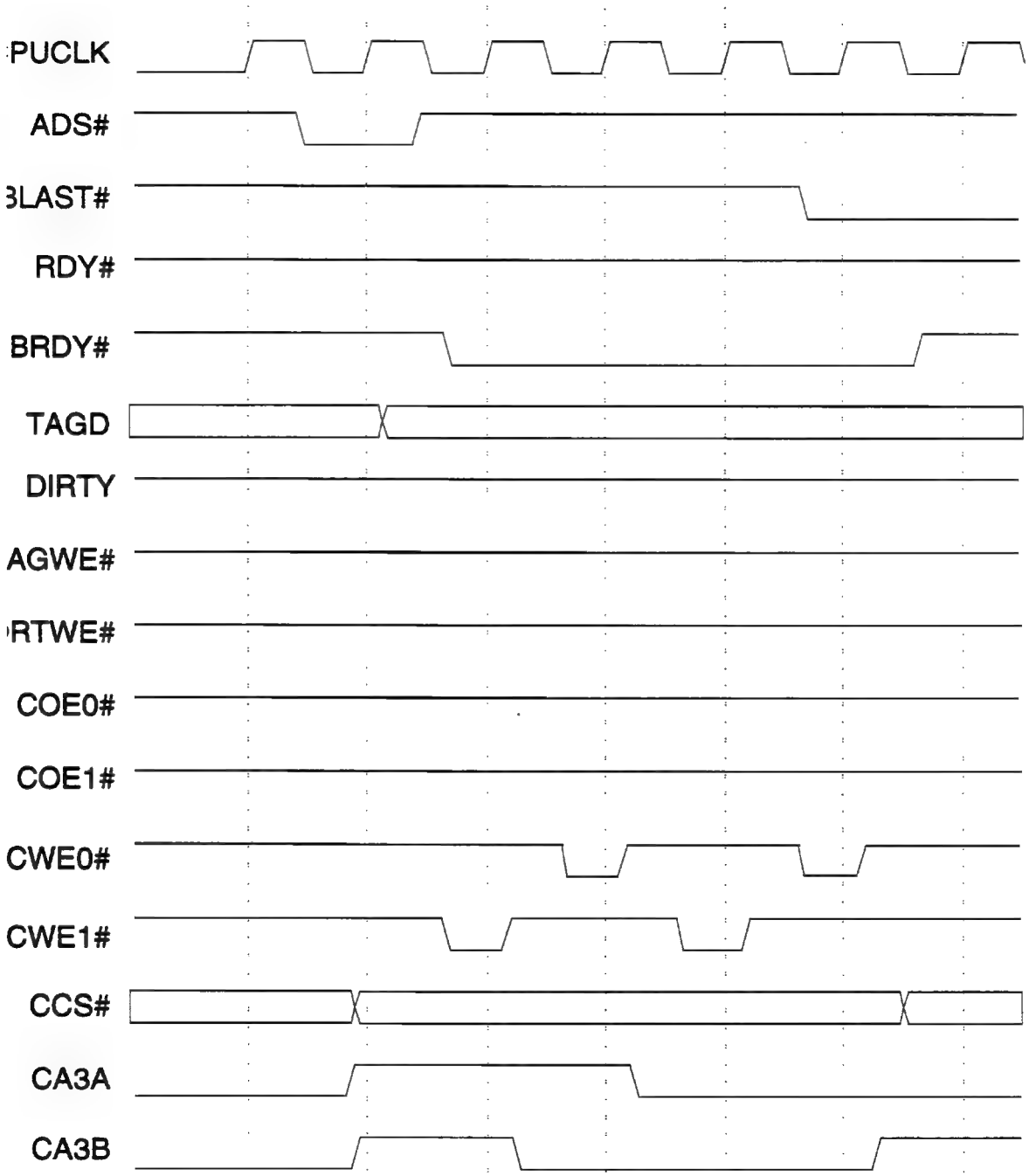
7.2.7 L2 Cache Read Hit dual bank interleave 2-2-2-2 cycle



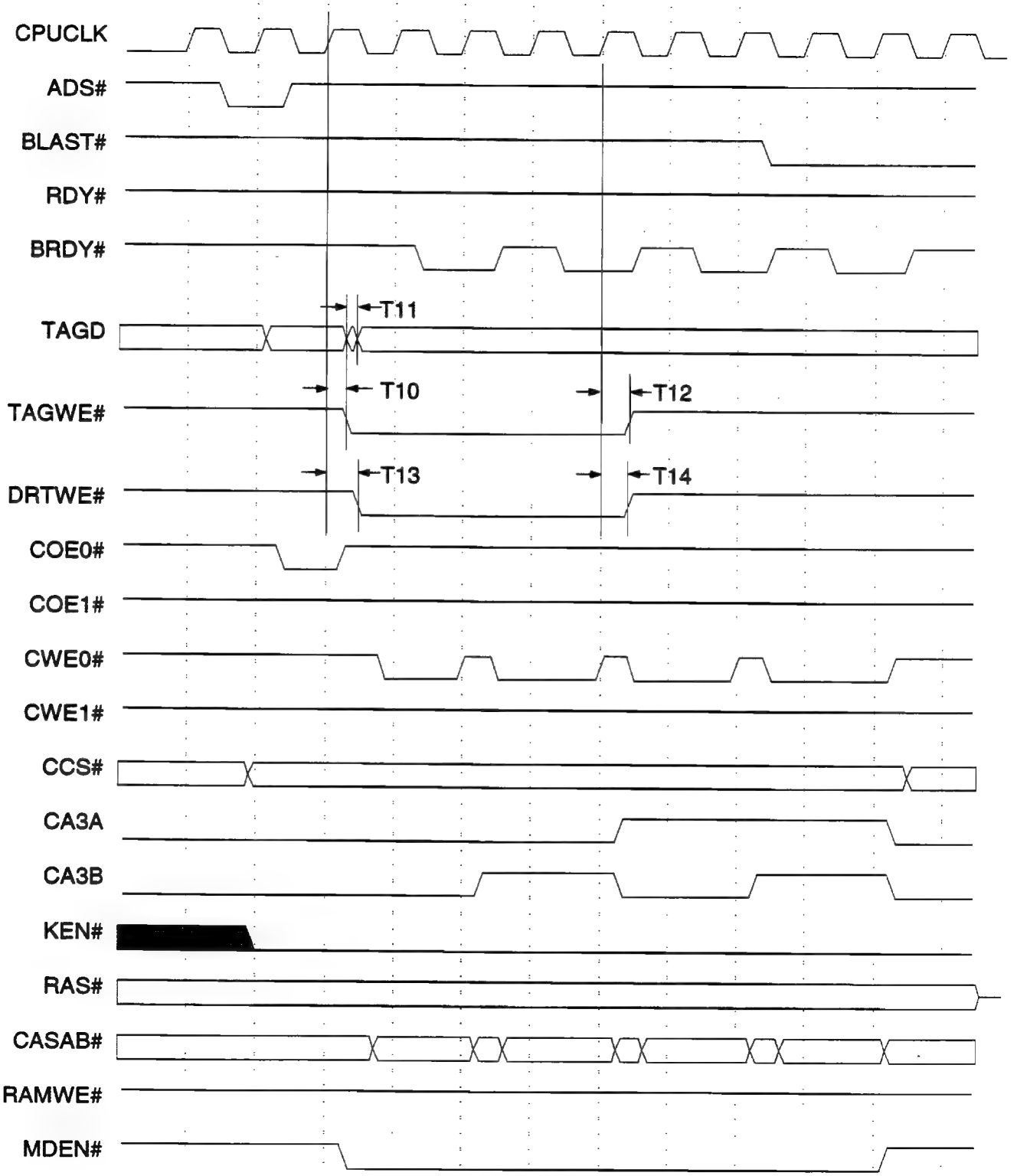
7.2.8 L2 Cache Write Hit dual bank interleave 3-1-1-1 cycle



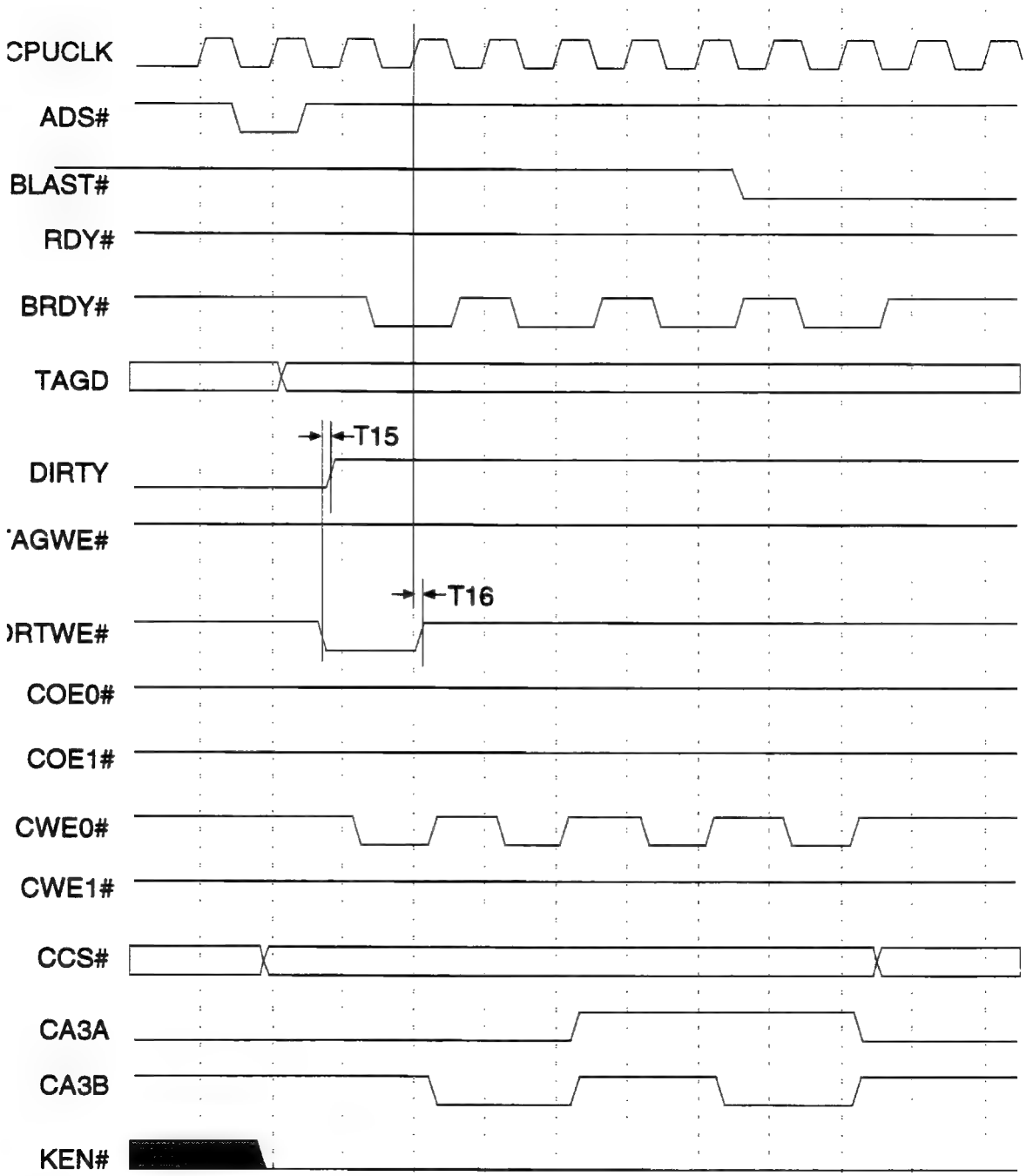
7.2.9 L2 Cache Write Hit dual bank interleave 2-1-1-1 cycle write back



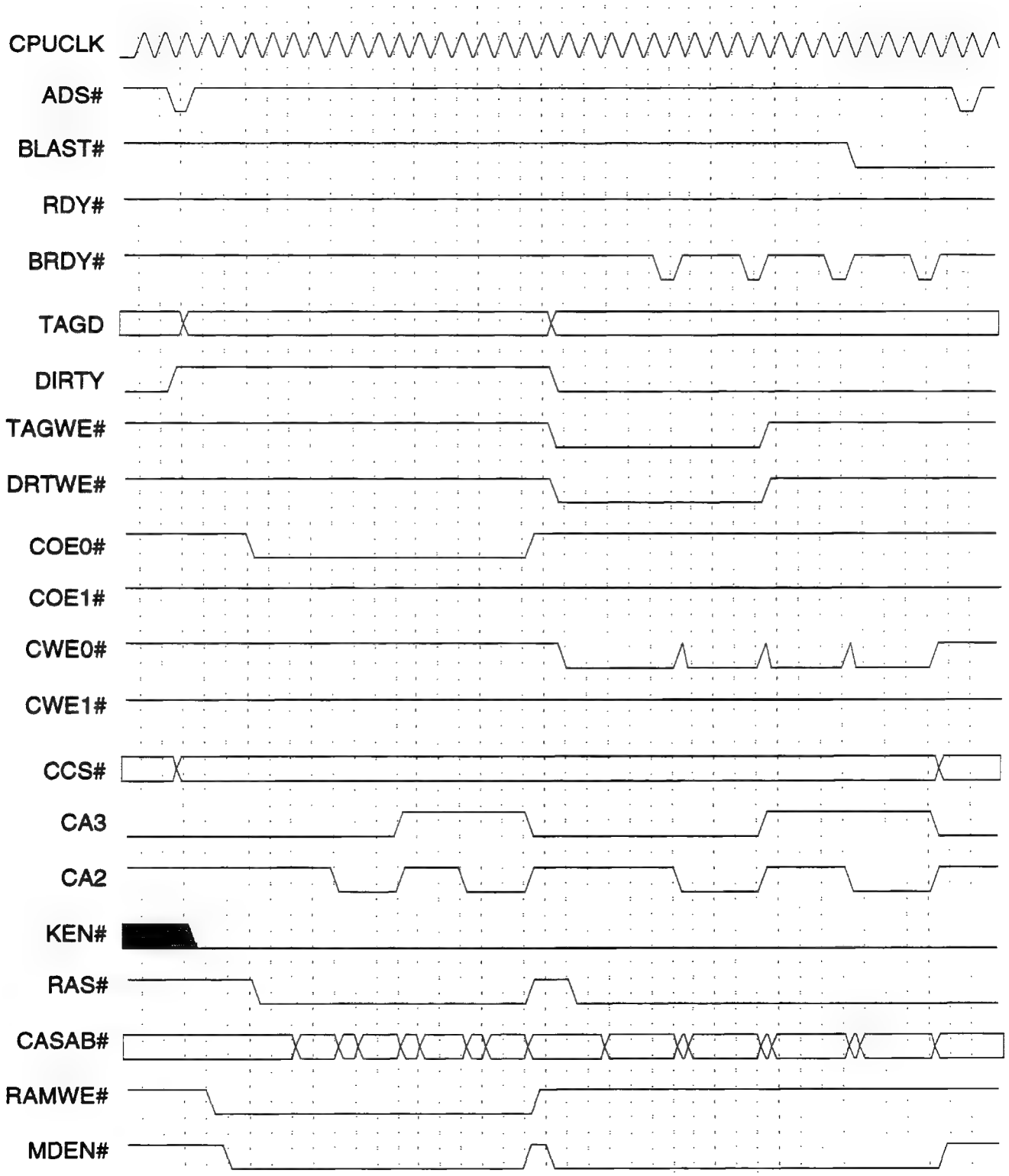
7.2.10 Clean Line Replacement single bank non-interleave mode



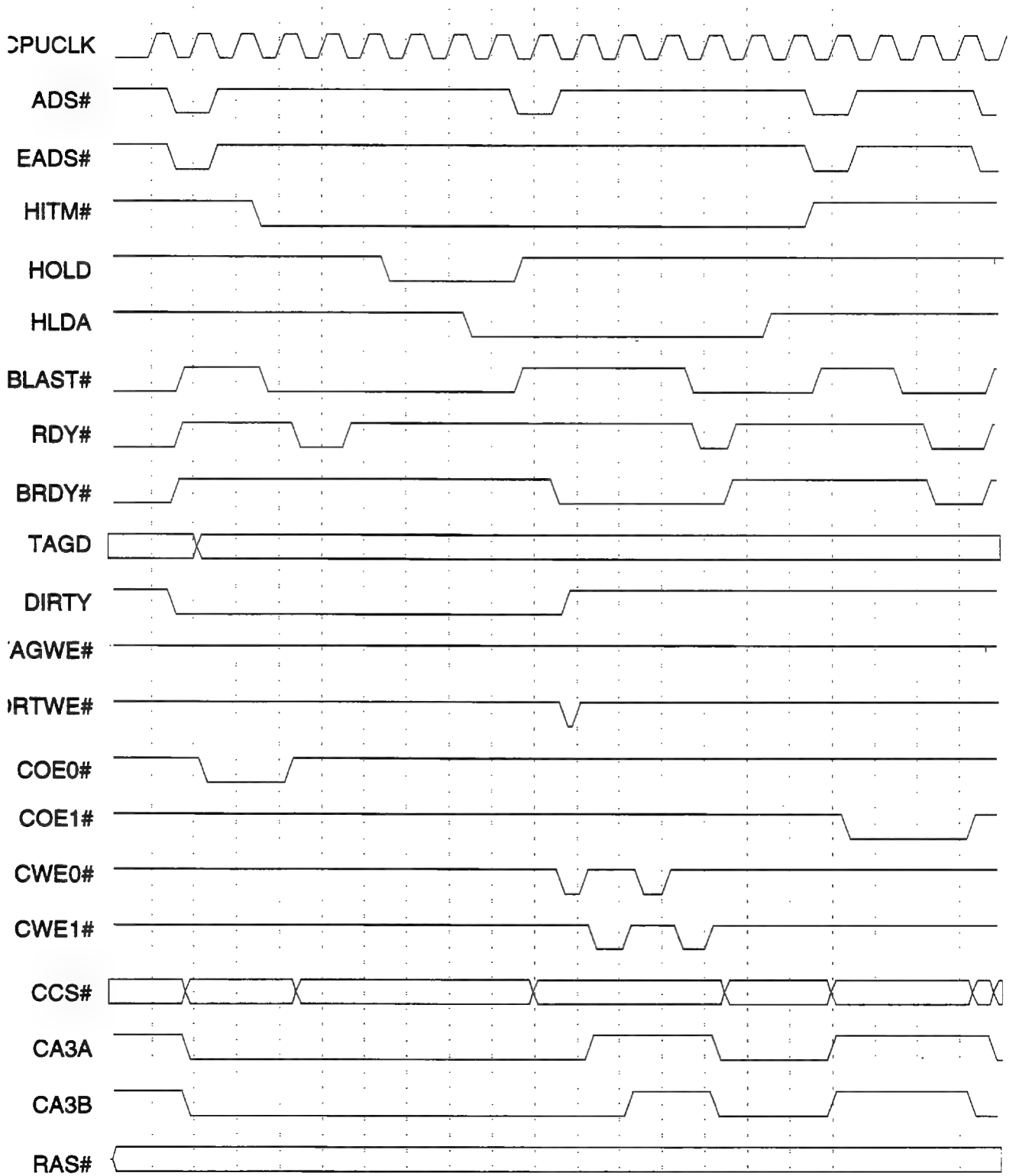
7.2.11 L2 Cache Write Hit clean line update to dirty single bank



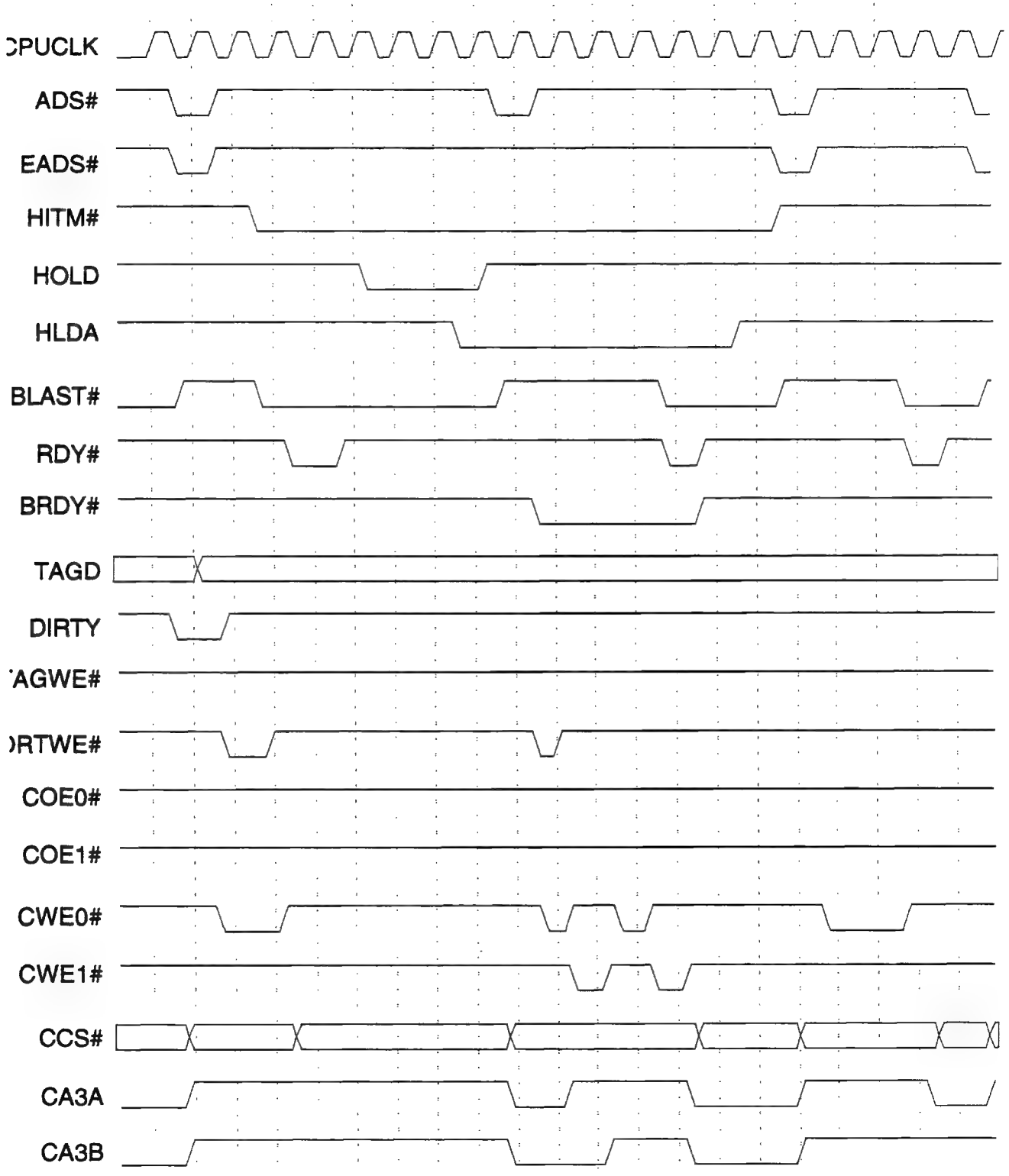
7.2.12 Dirty Line Copy Back replacement single bank mode



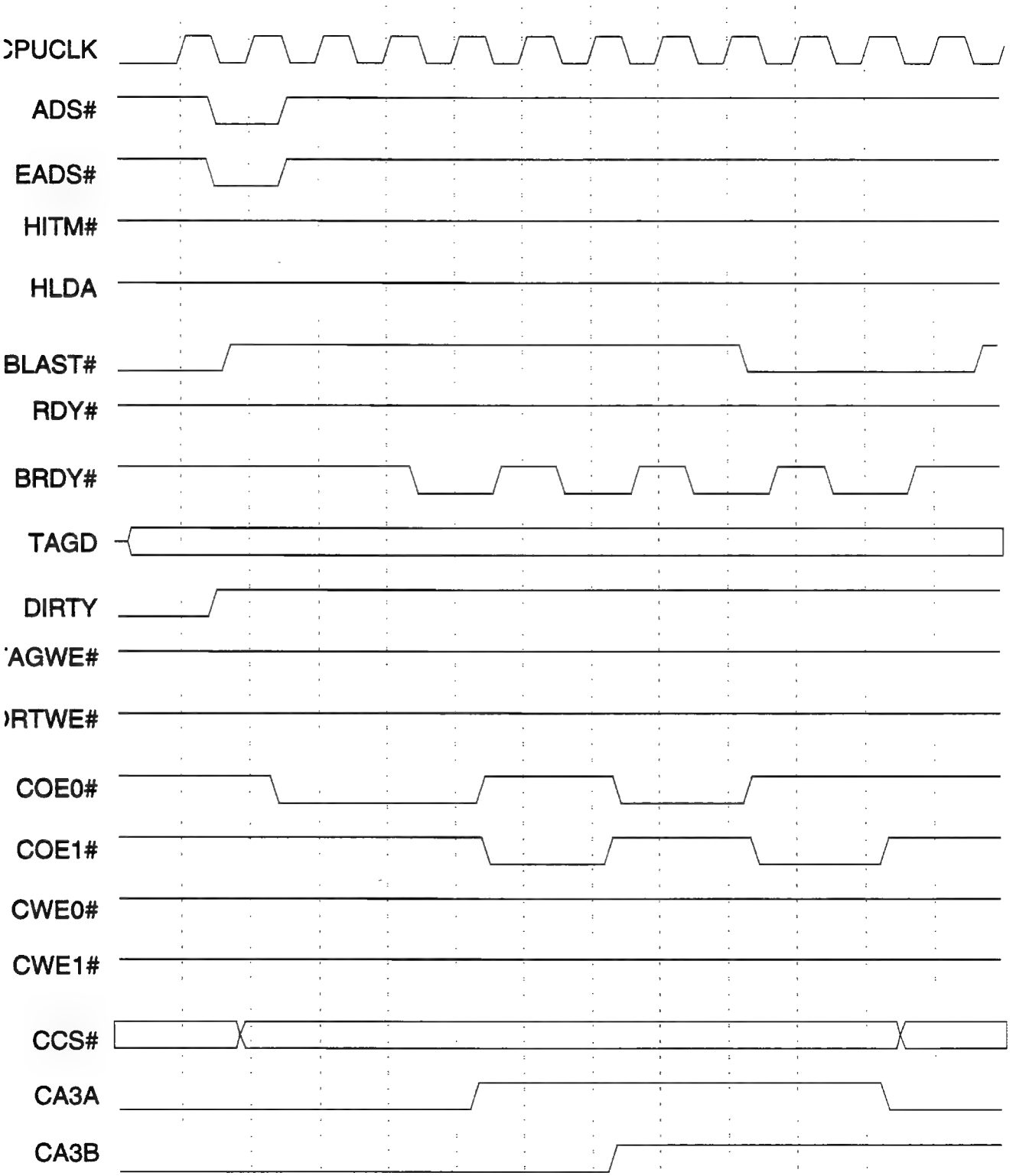
7.2.13 L2 Cache Read Hit VL Master *CPU intervene*



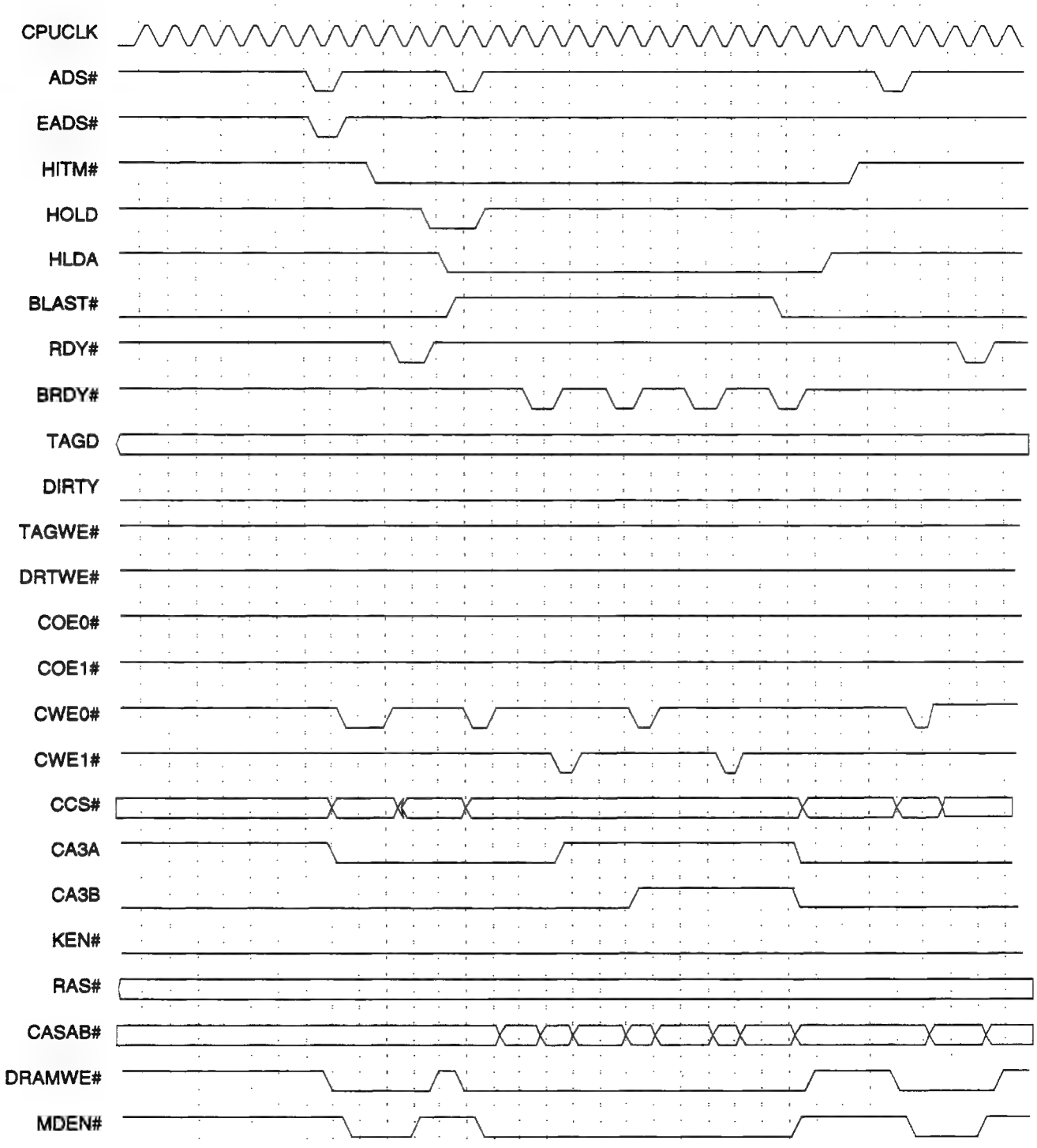
7.2.14 L2 Cache Write Hit LV Master *CPU intervene*



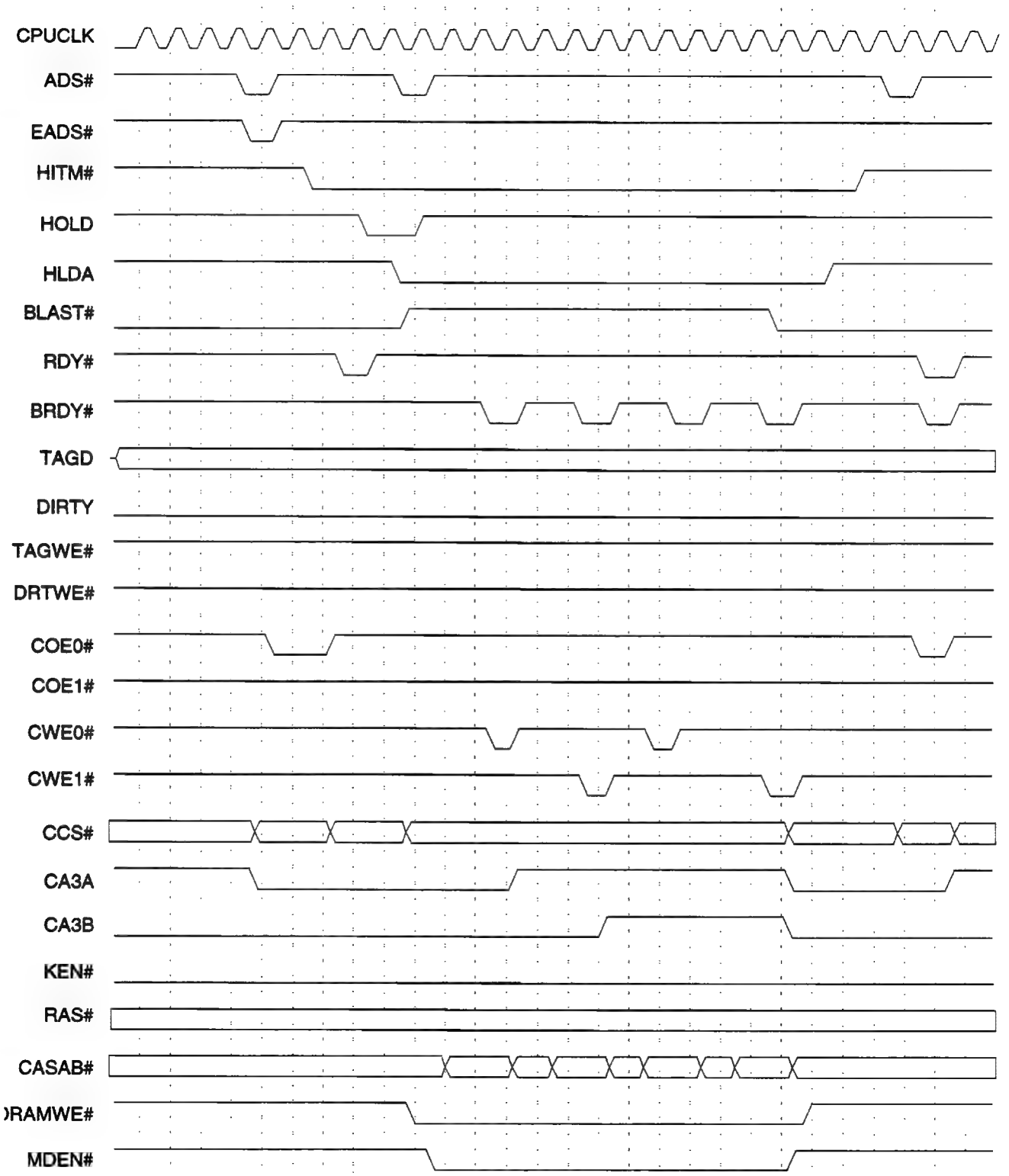
7.2.15 L2 Cache Burst Read Hit VL Master *no CPU intervene*



7.2.16 L2 Cache Write Hit ISA DMA Cycle *CPU intervene*

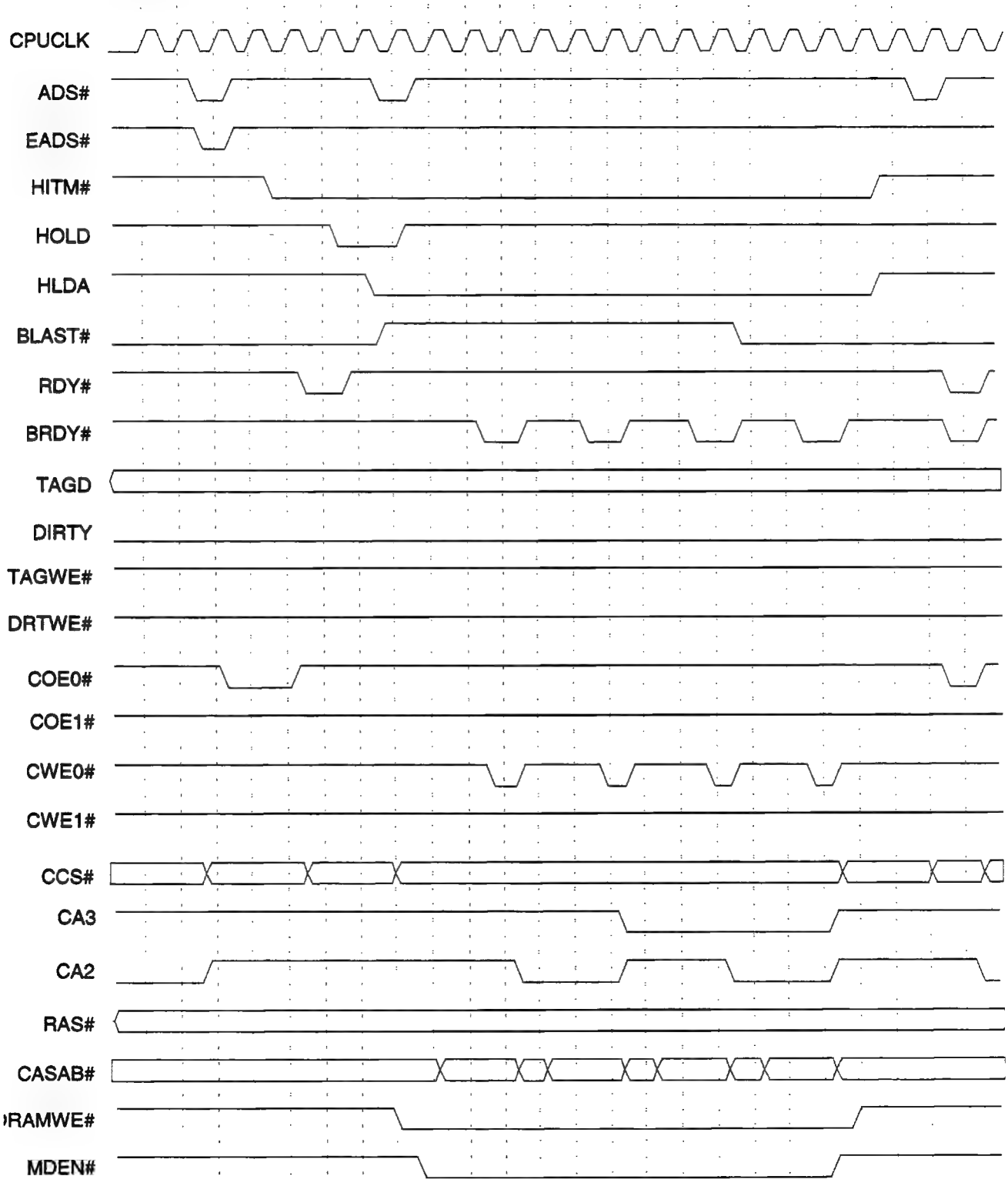


7.2.17 L2 Cache Read Hit ISA DMA Cycle
CPU intervene dual bank interleave

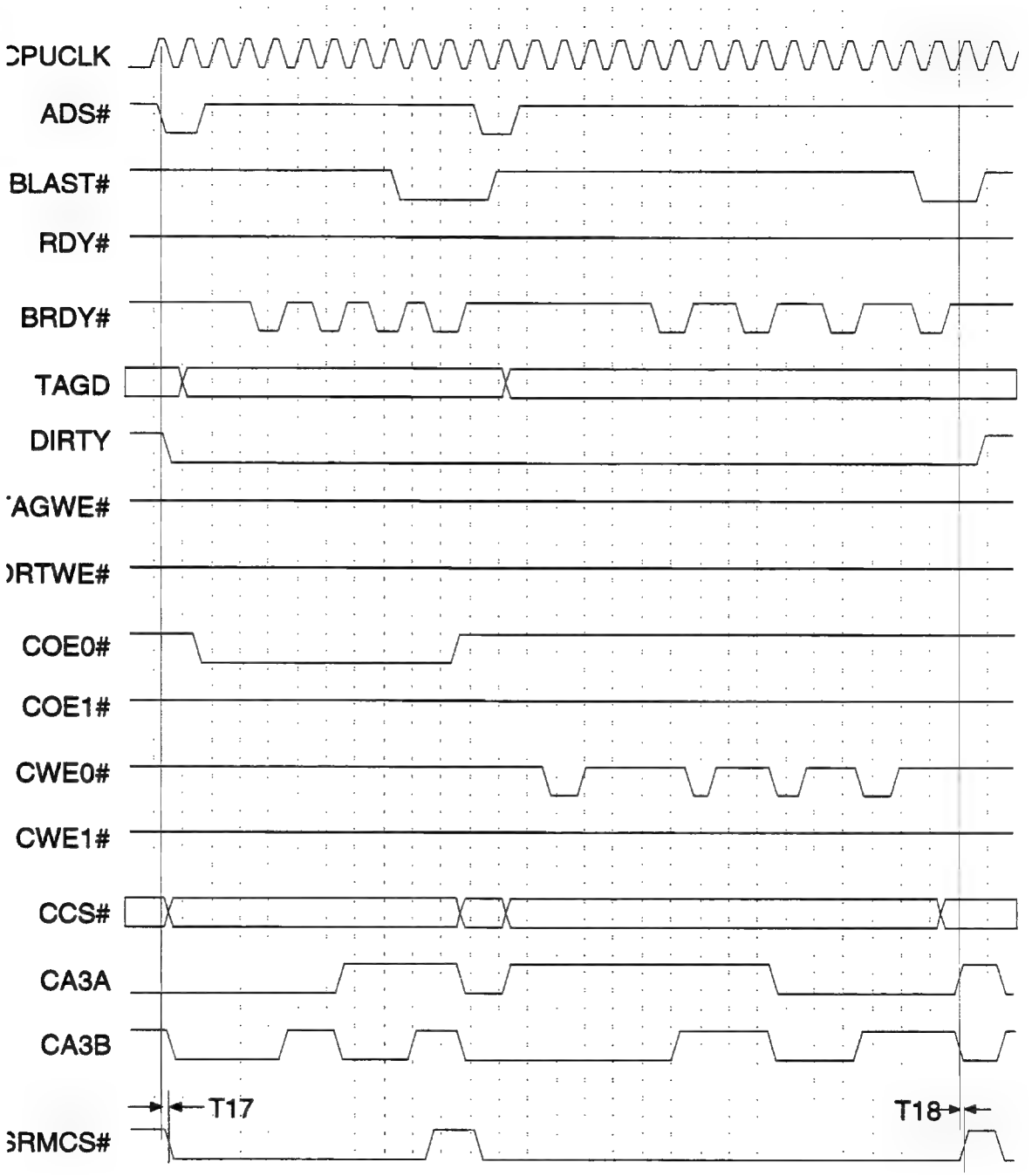


7.2.18 L2 Cache Read Hit ISA Bus Master

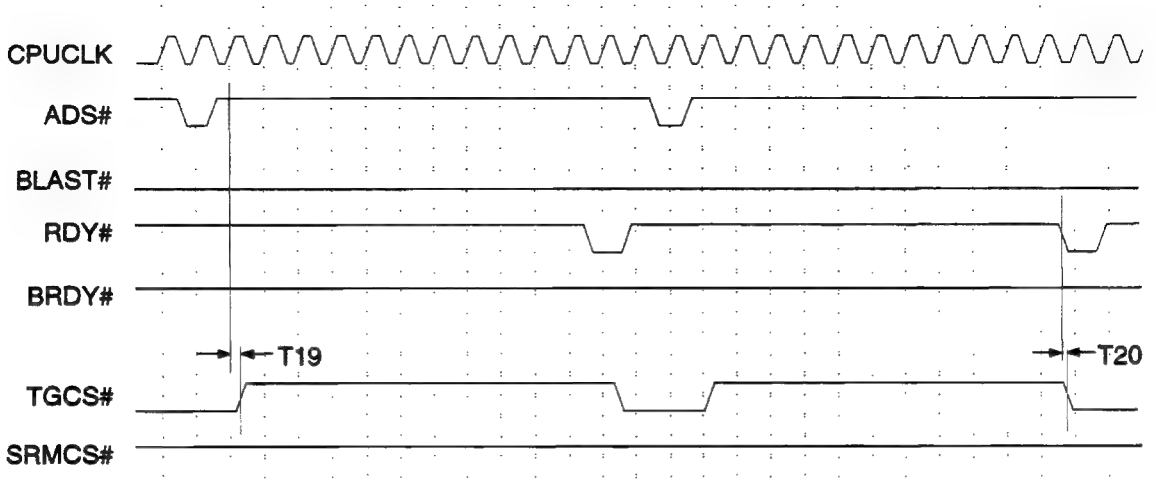
CPU intervene single bank



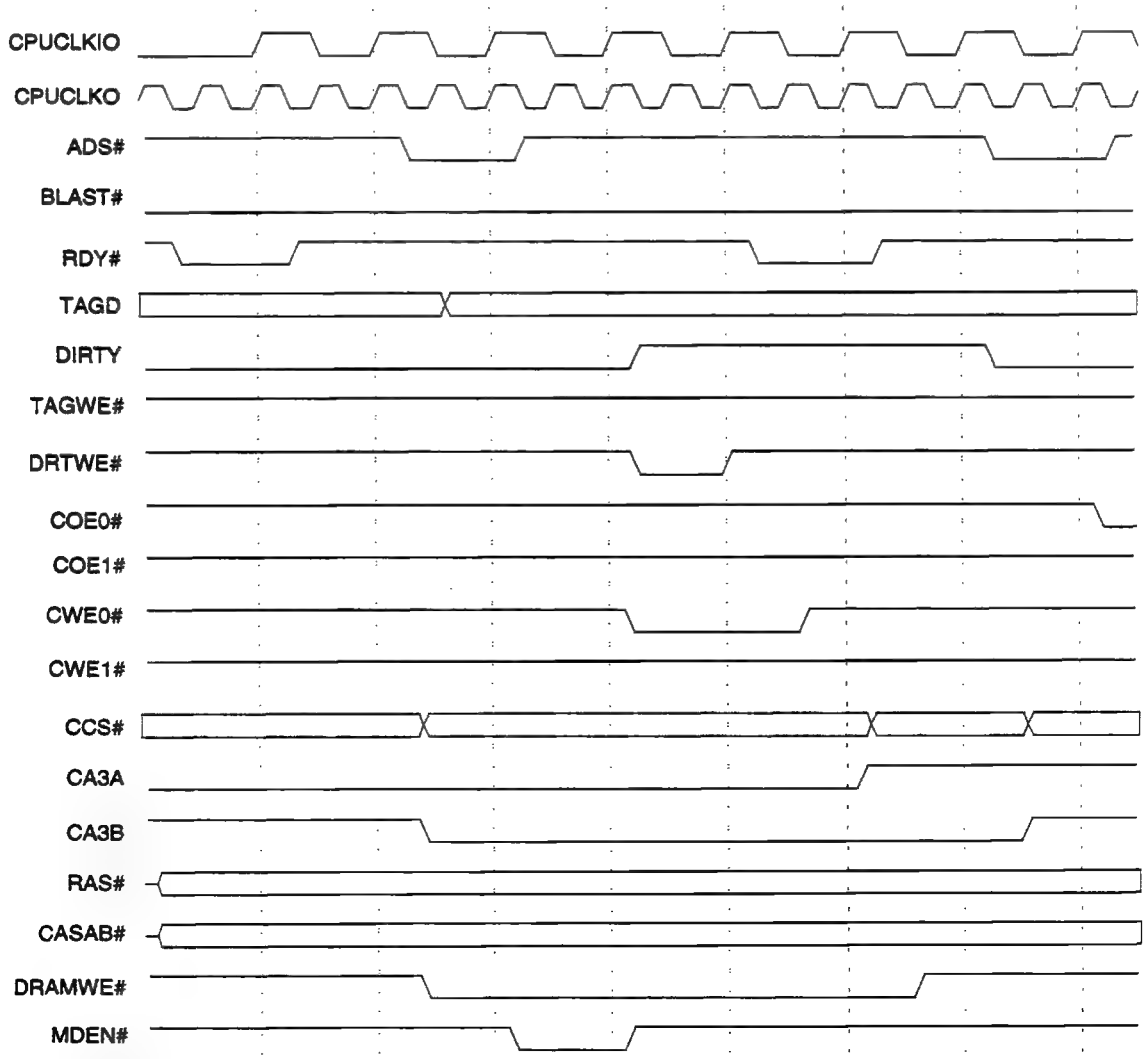
7.2.19 SRMCS# Signal Timing During Cache Cycles



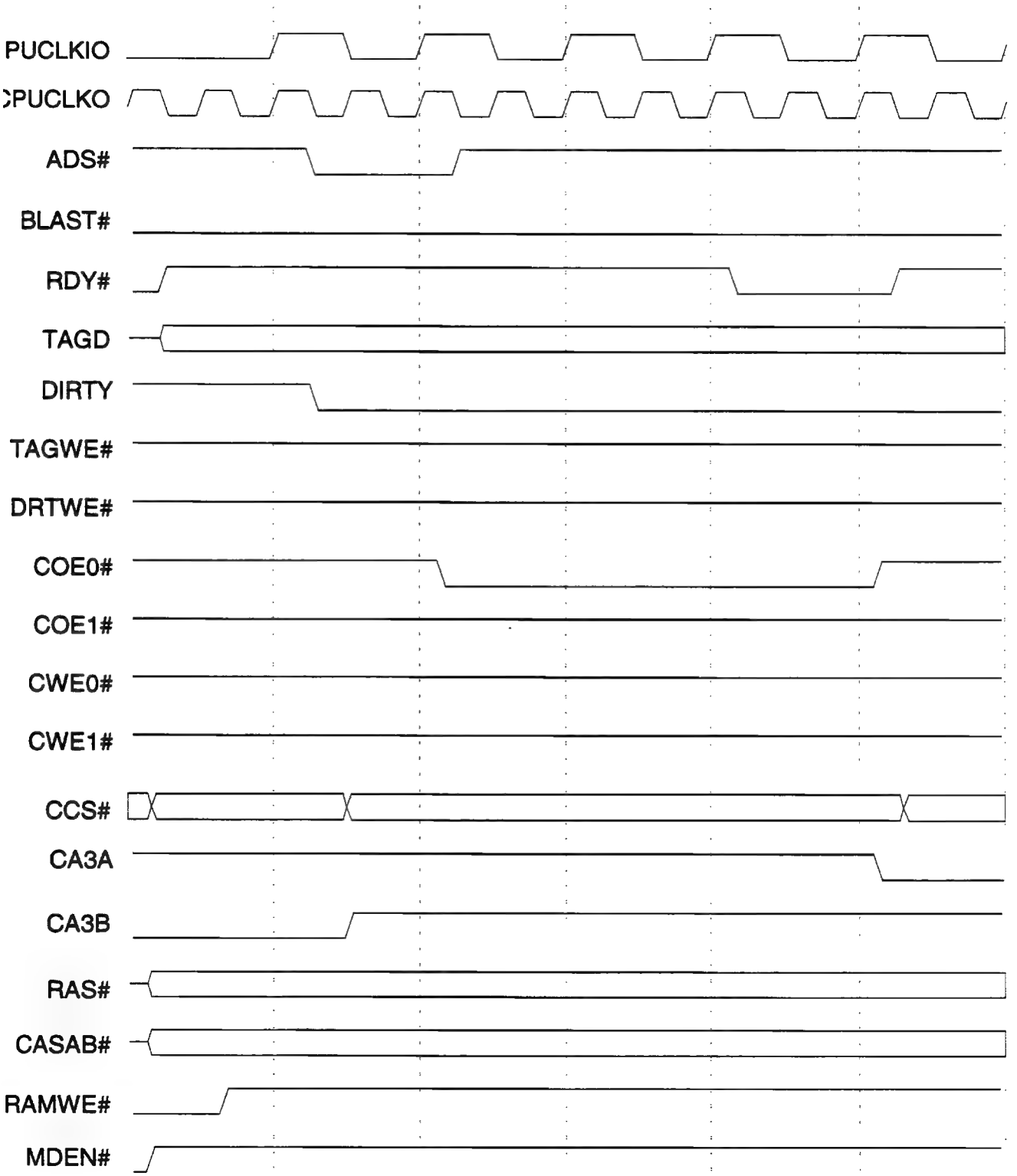
7.2.20 TGCS# Signal Timing During Cache and Other Cycles



7.2.21 386 (2x) Clock Mode L2 Cache Write Hit

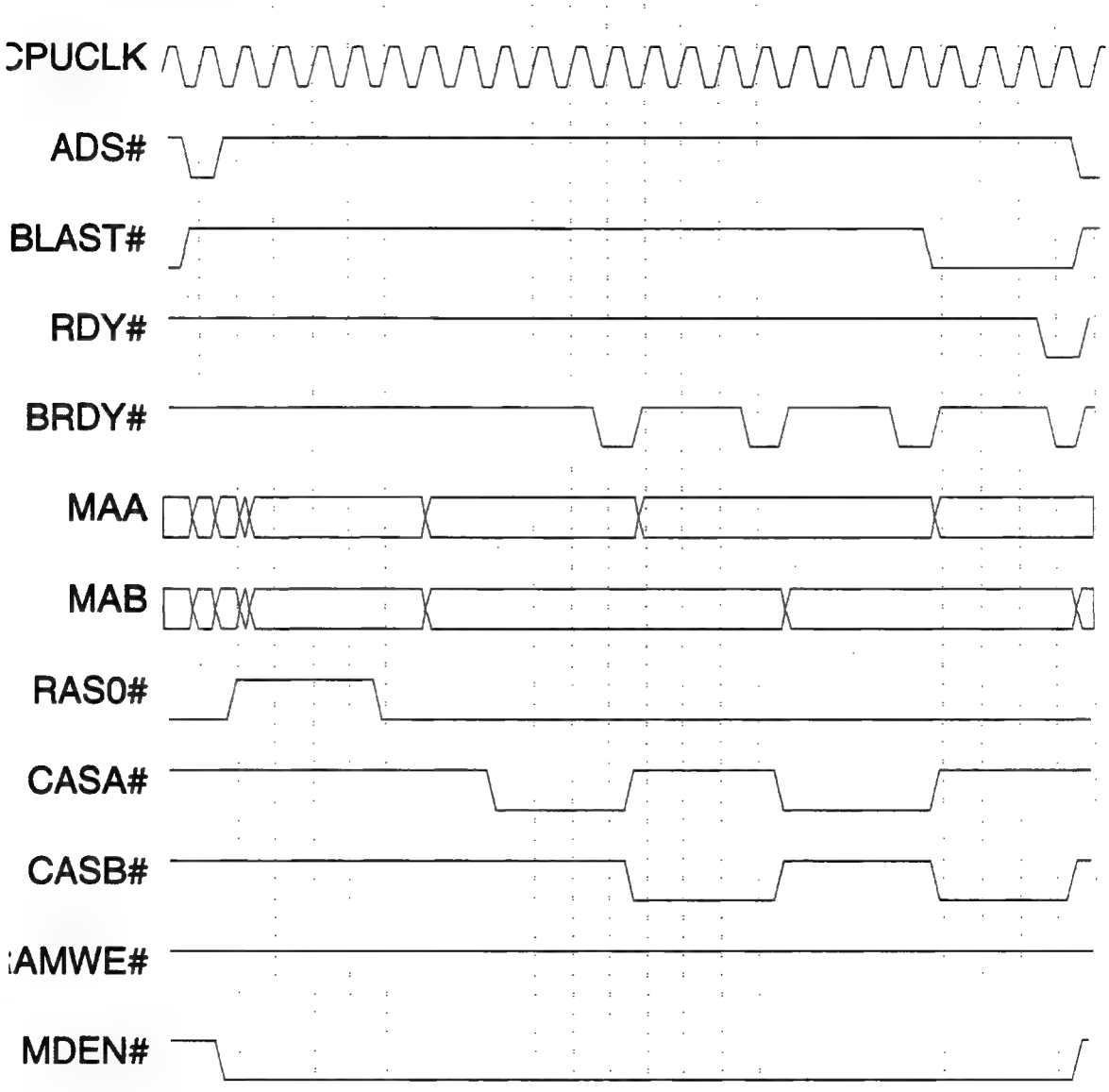


7.2.22 L2 Cache Read Hit 386 (2x) Clock Mode

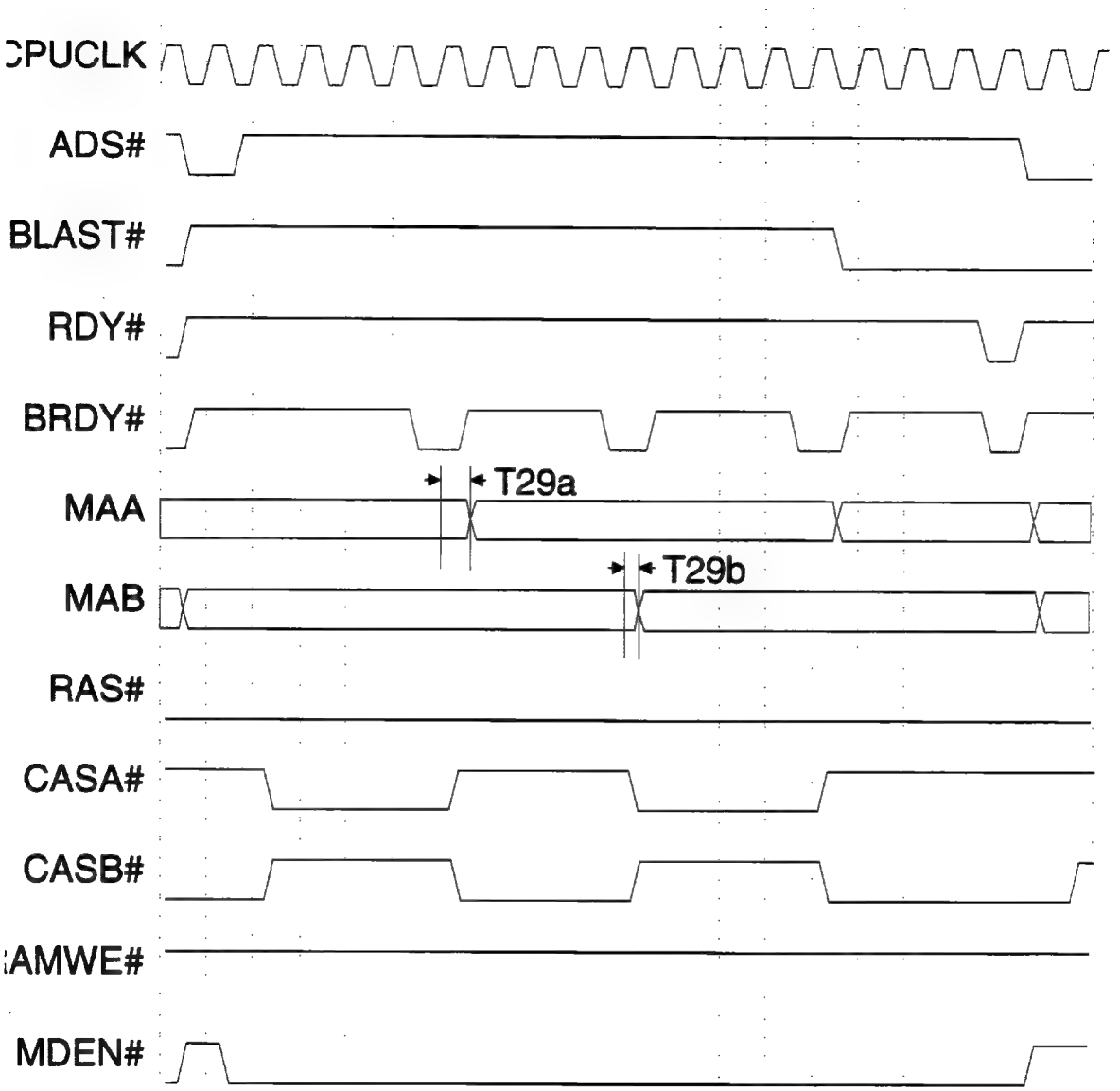


7.3 DRAM Interface

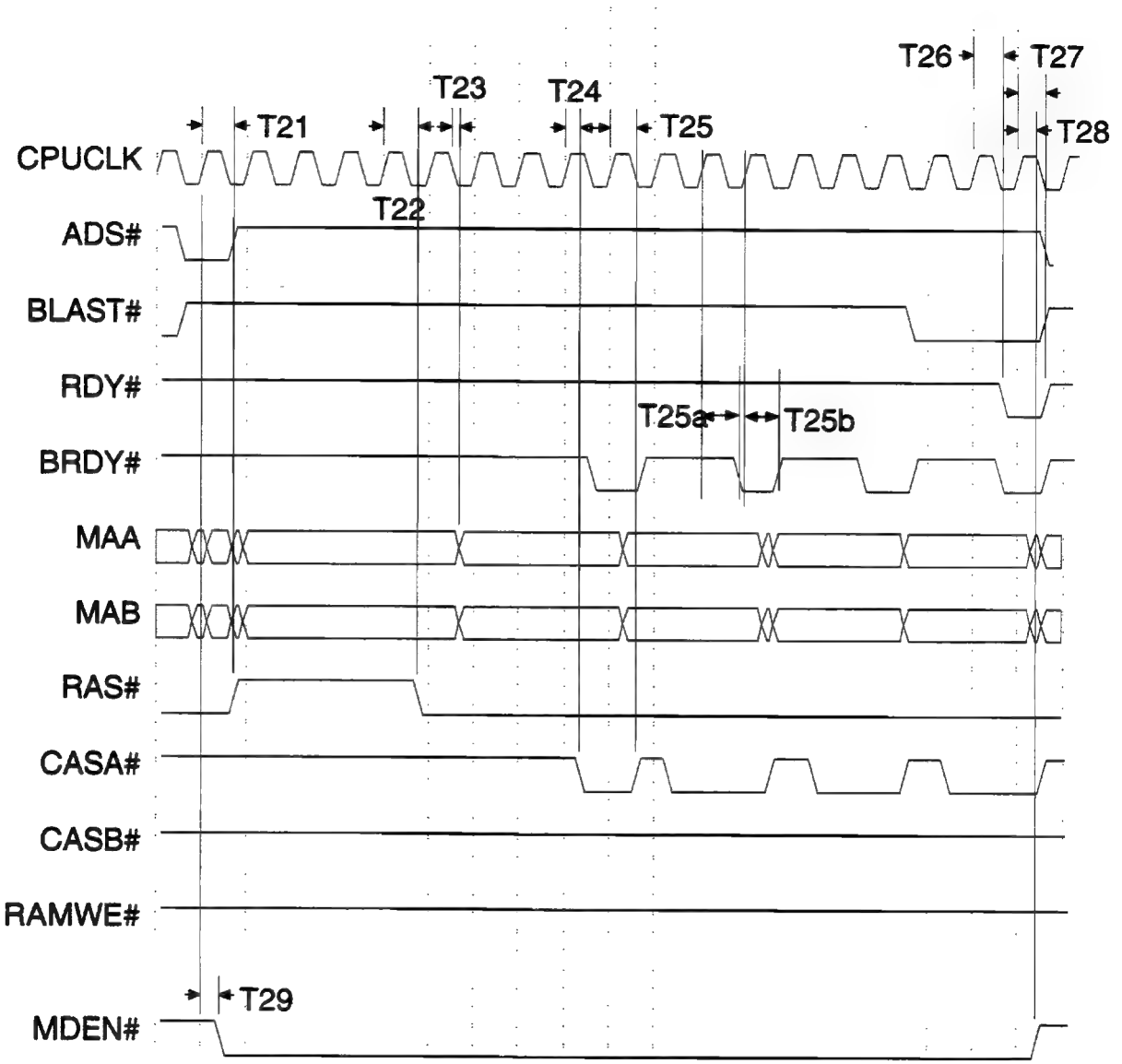
7.3.1 Read Page Miss Interleave



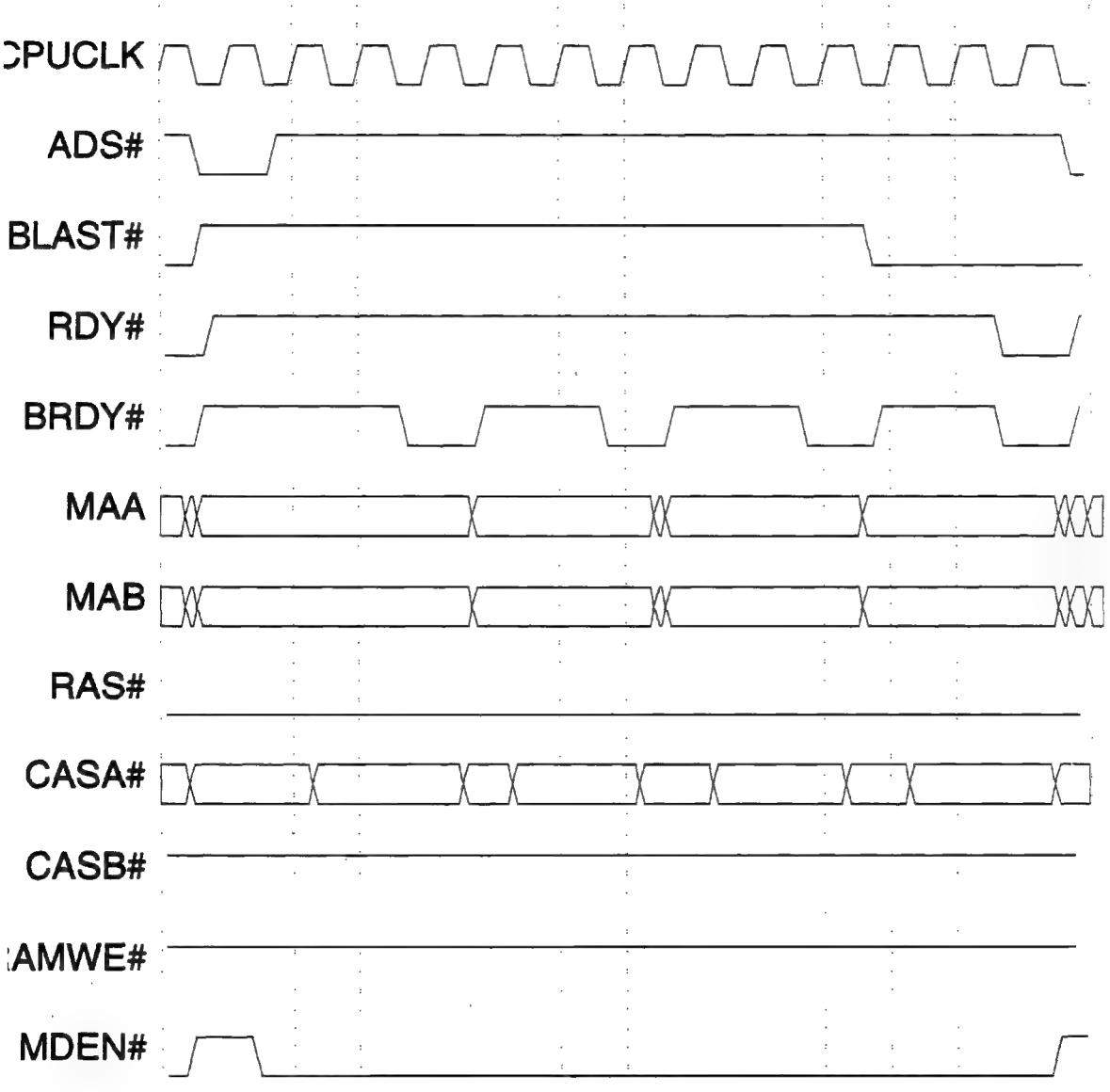
7.3.2 Read Page Hit Interleave



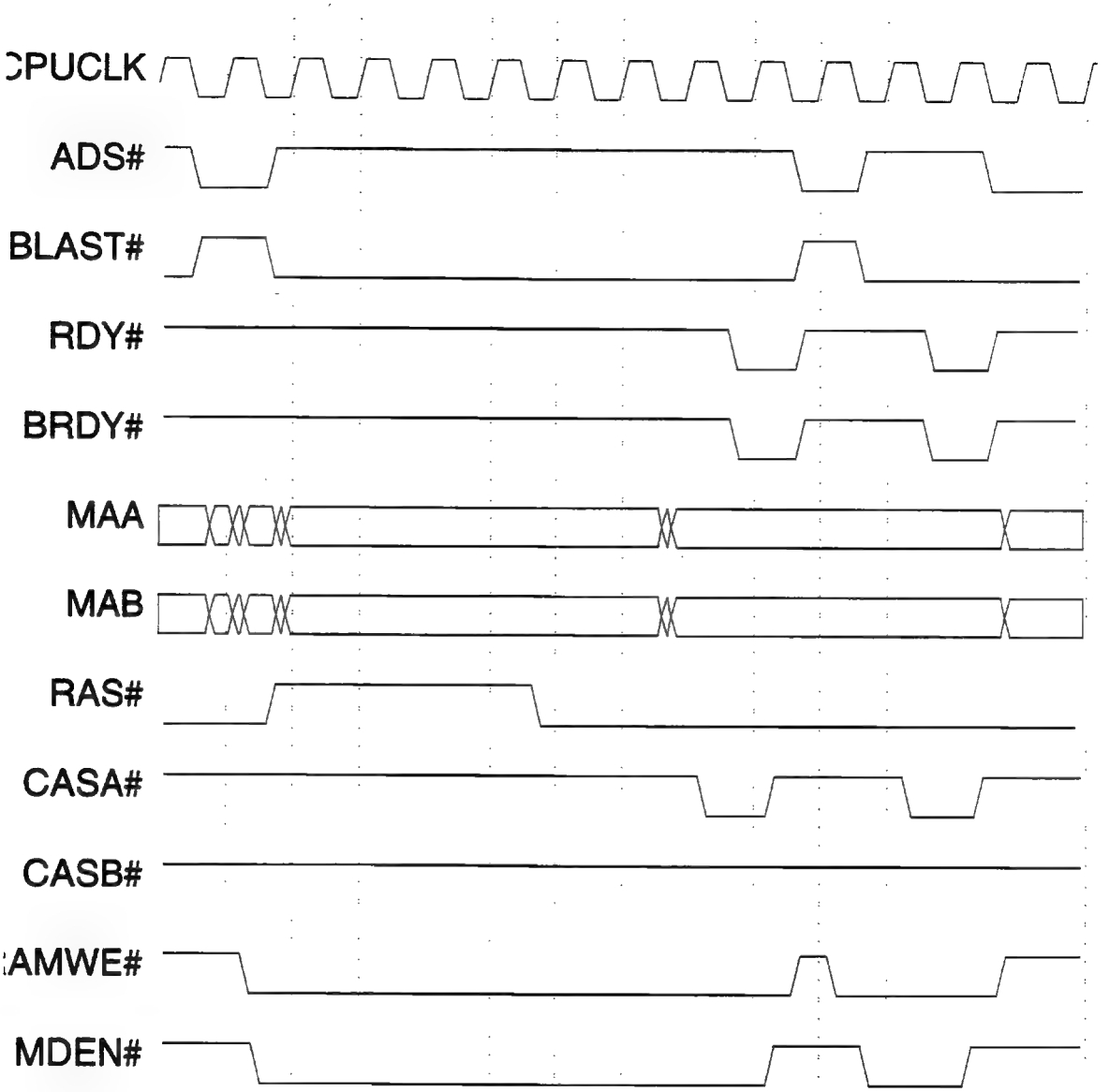
7.3.3 Read Page Miss Non-interleave



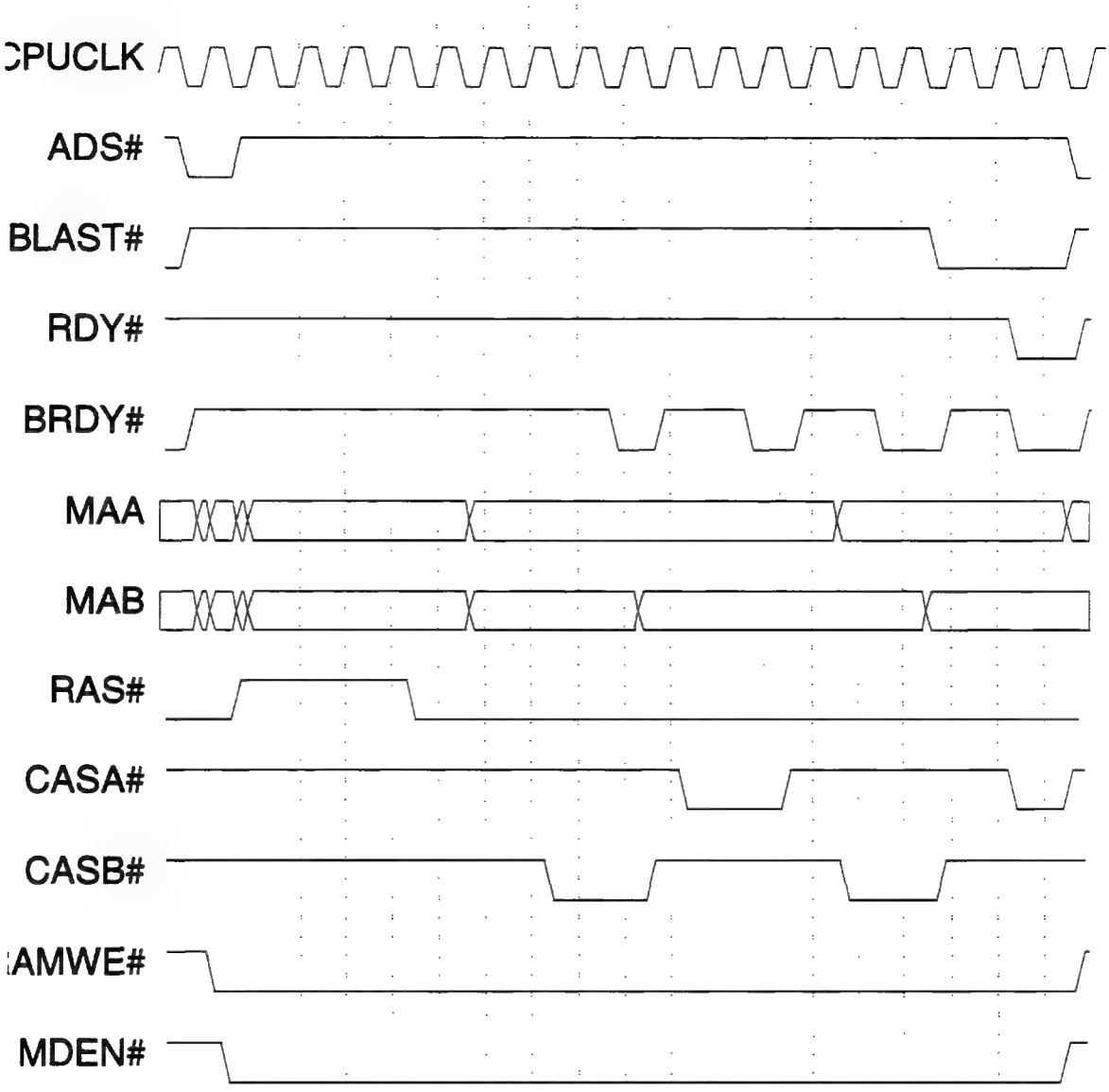
7.3.4 Read Page Hit Non-interleave



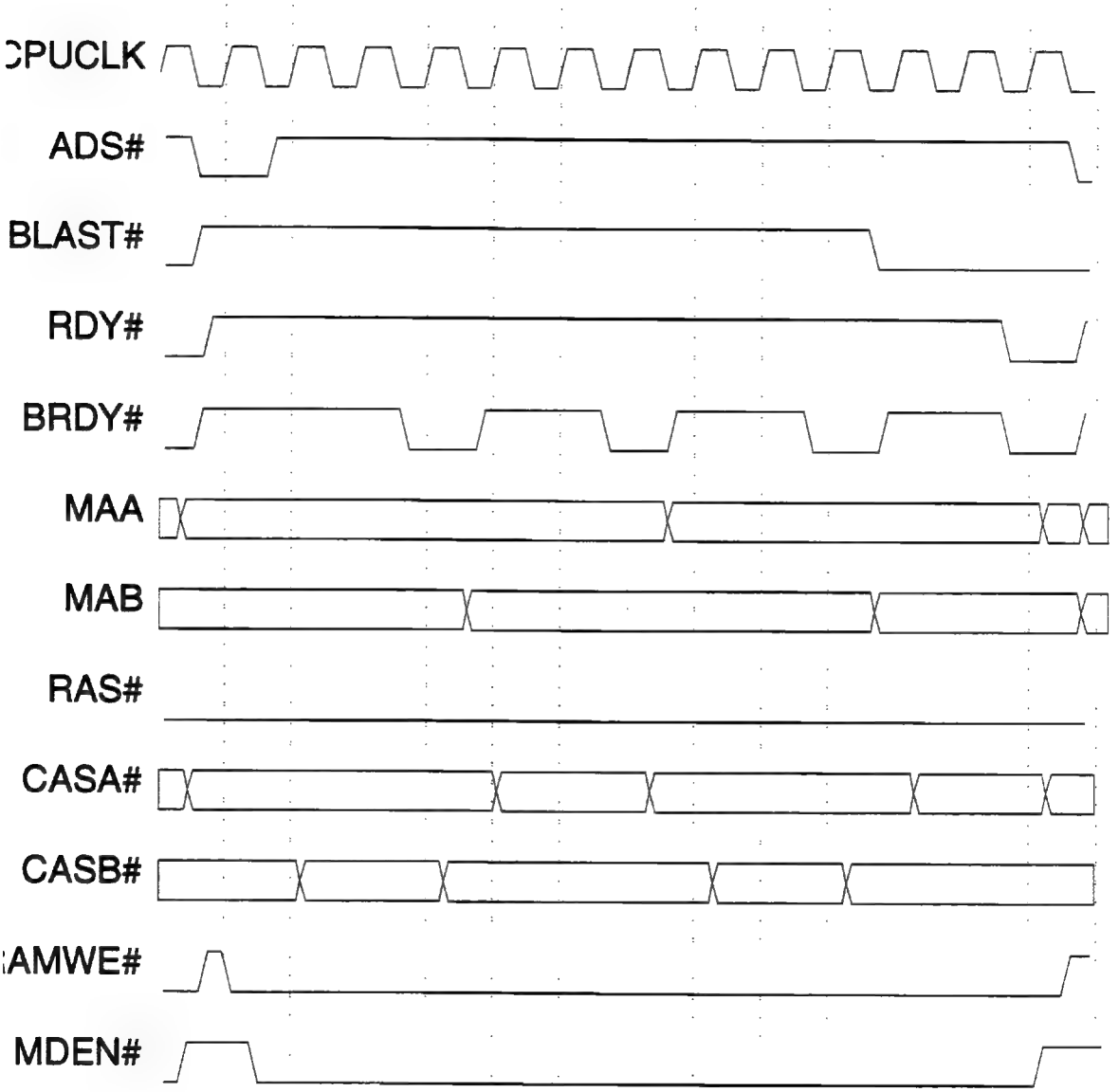
7.3.5 Write Page Miss ↔ Write Page Hit Non-interleave



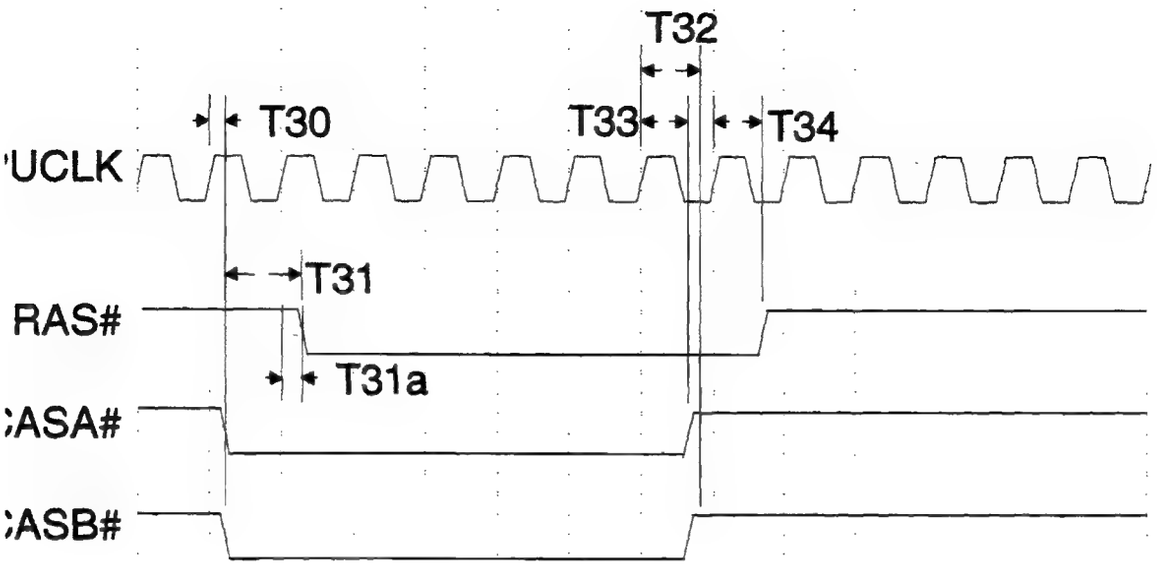
7.3.6 Write Page Miss Interleave



7.3.7 Burst Write Hit Interleave



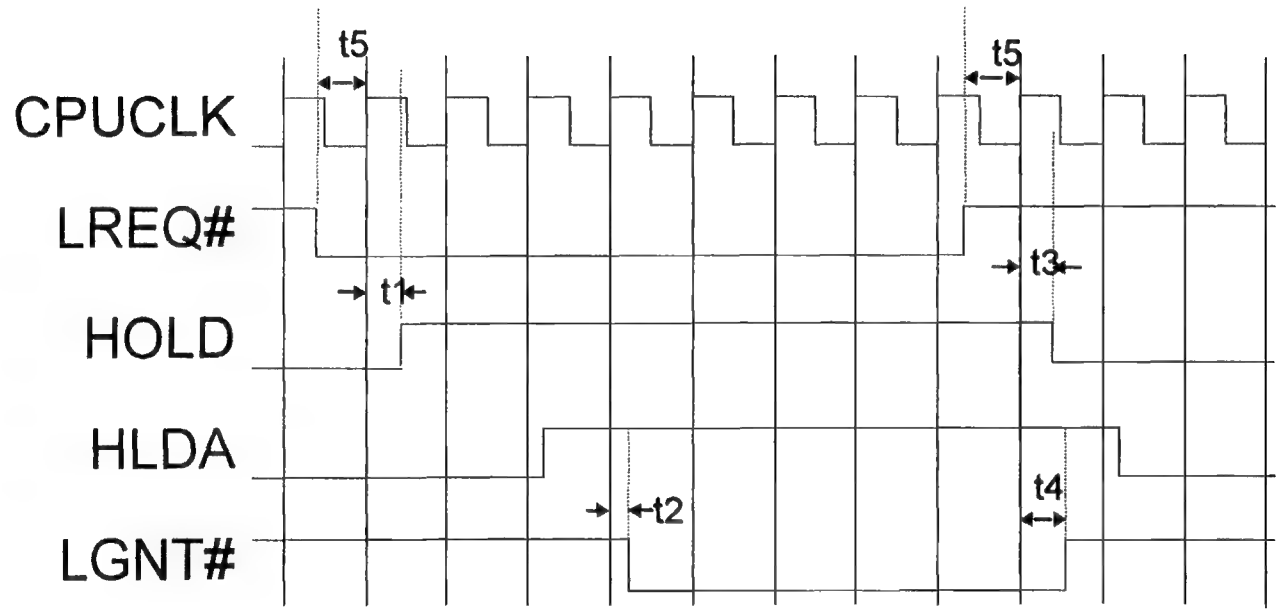
7.3.8 DRAM Refresh Normal



7.4 VESA Bus Interface

TBD

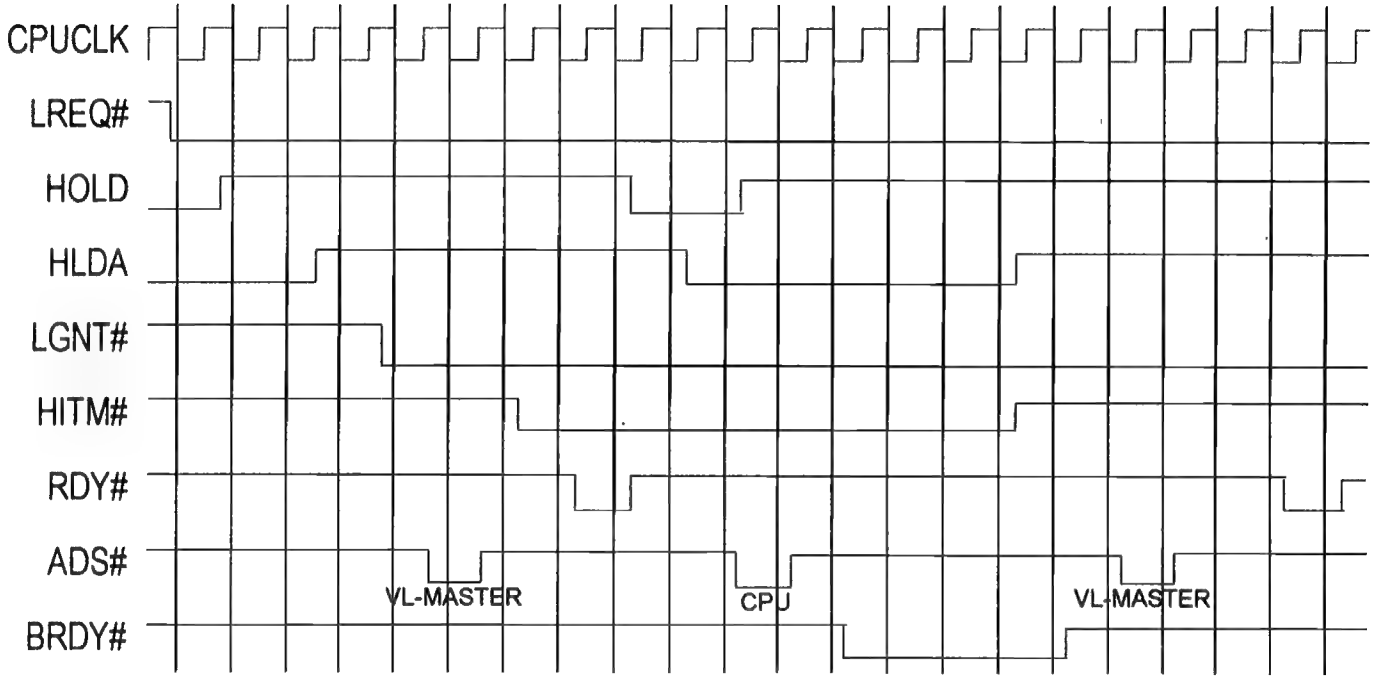
VL BUS TIMING



t5: LREQ# setup time min 5ns

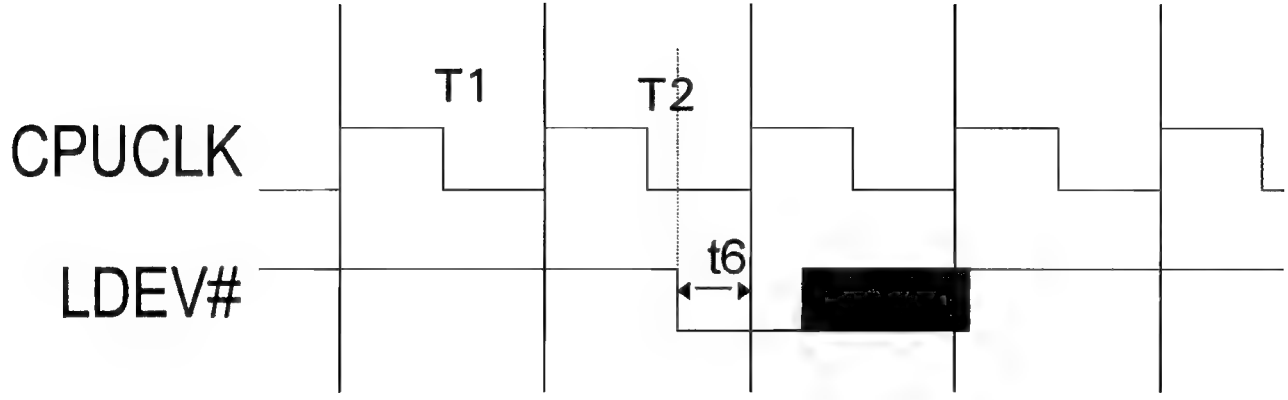
VL - MASTER

VL BUS TIMING



VL - MASTER + Hitm :

VL BUS TIMING

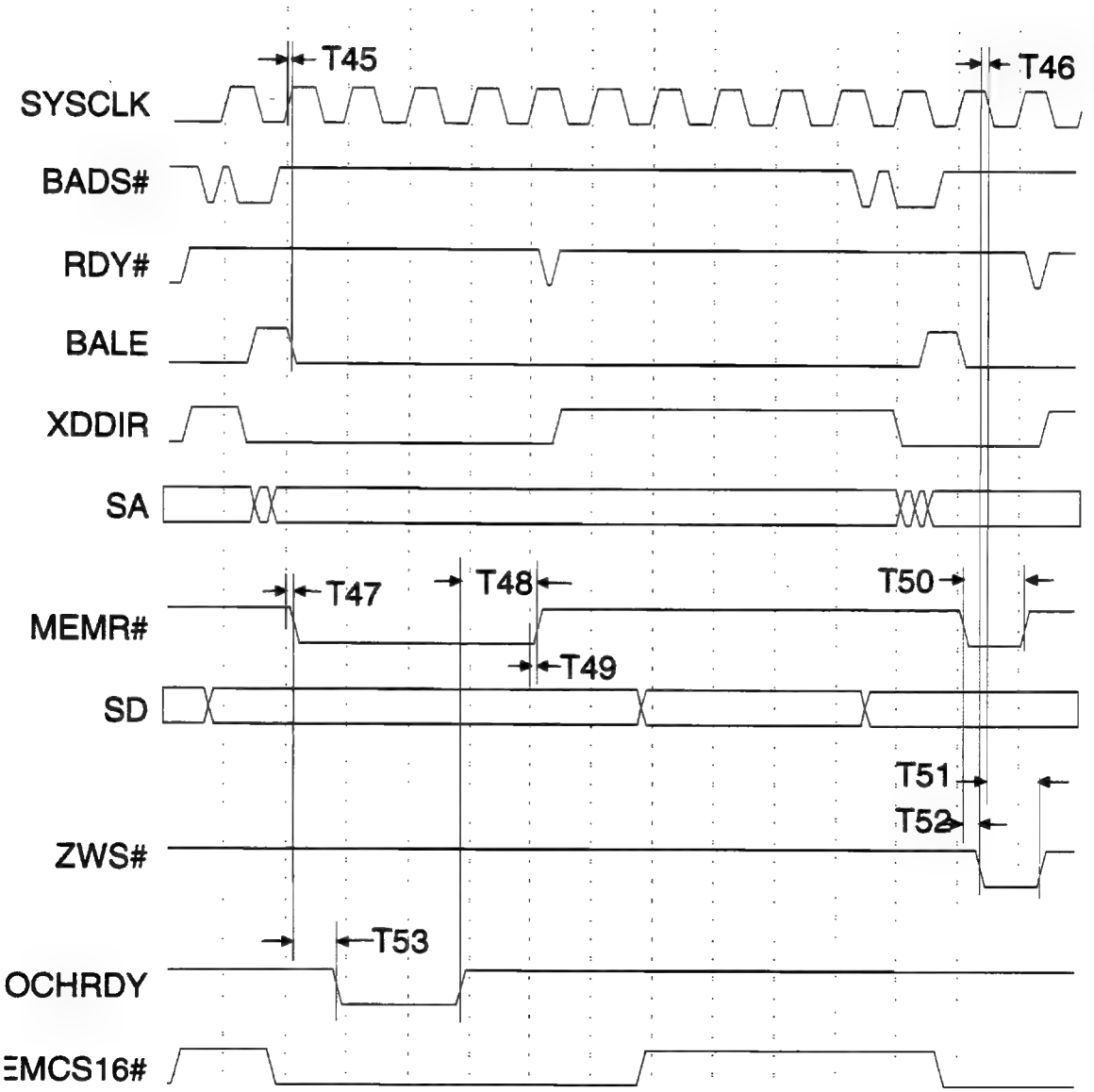


LDEV# setup time 5ns
This can be programmably either end of first T2 or end of second T2

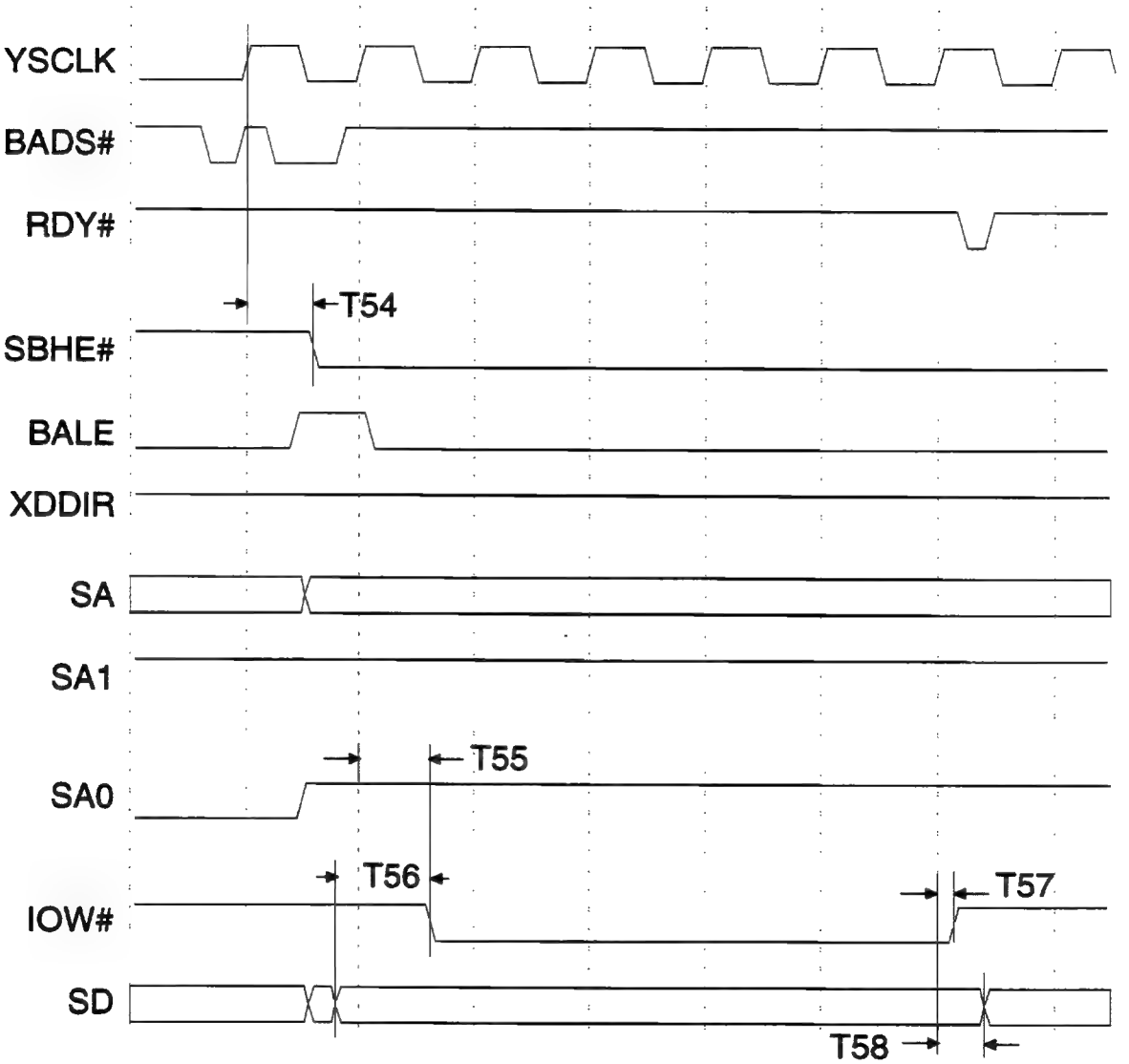
VL -SLAVE CYCLE

7.5 AT Bus Interface

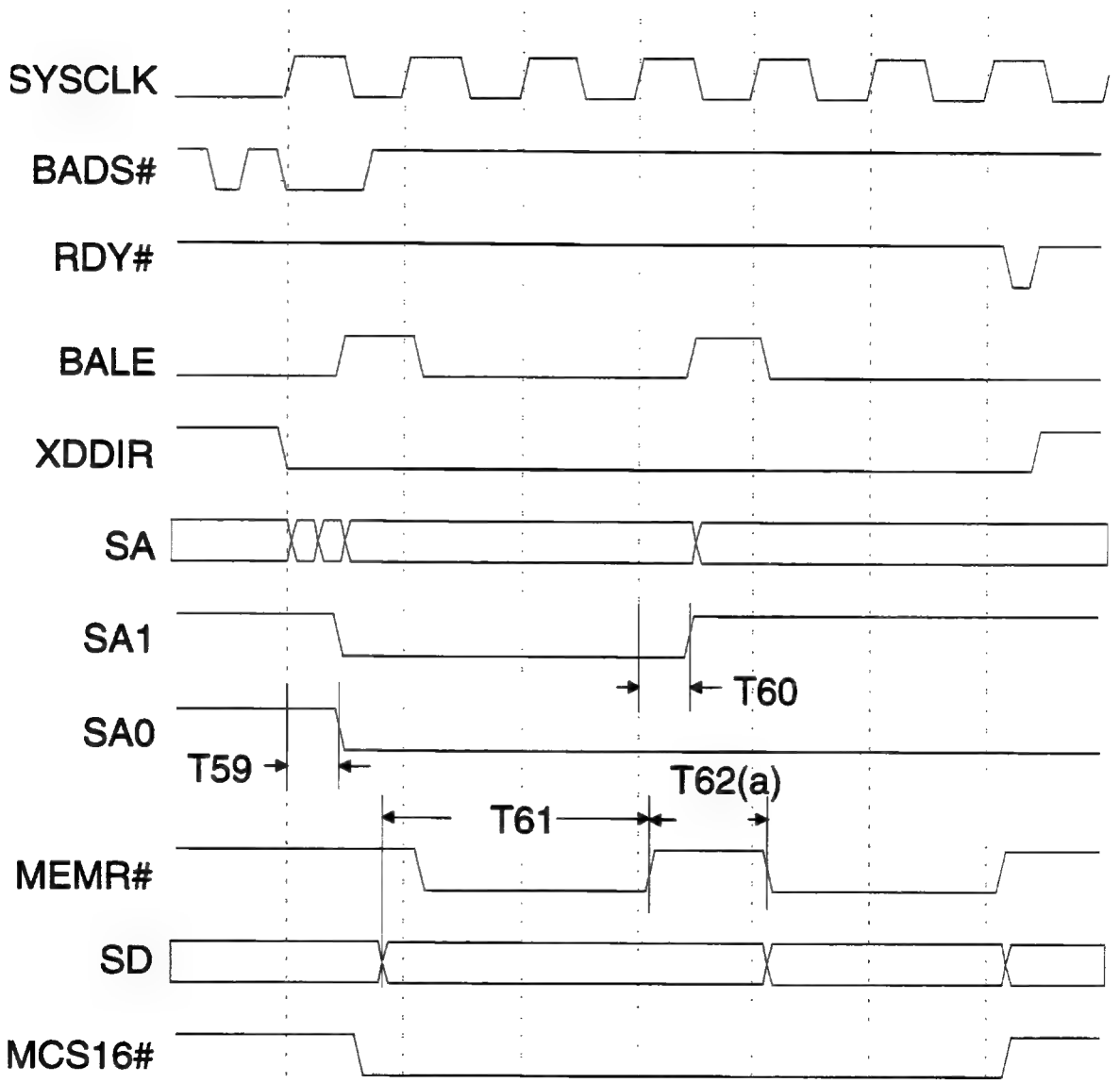
7.5.1 AT 16-bit Memory Read Cycle: IOCHRDY, zero WS



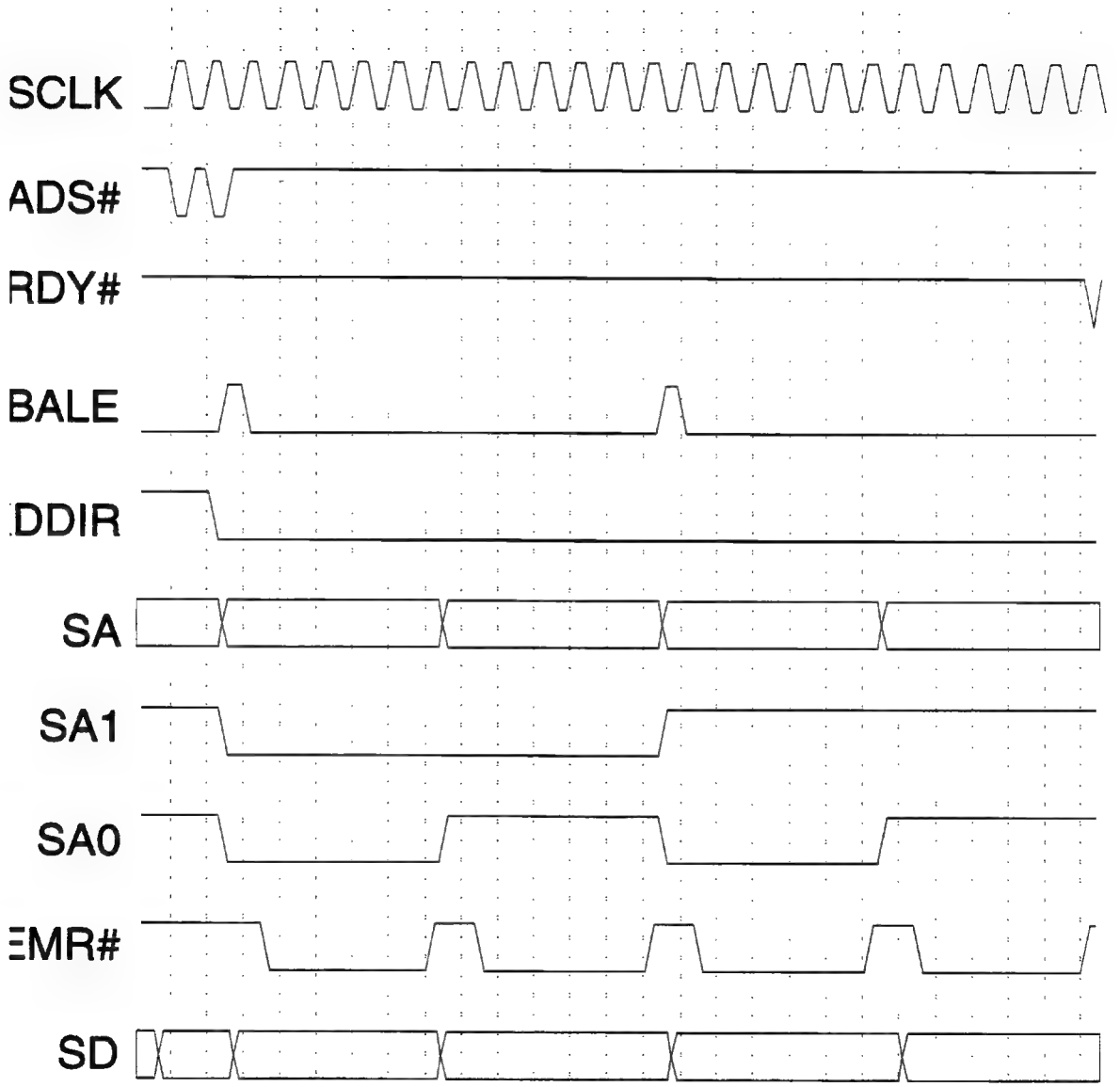
7.5.2 AT 8-bit IOW cycle



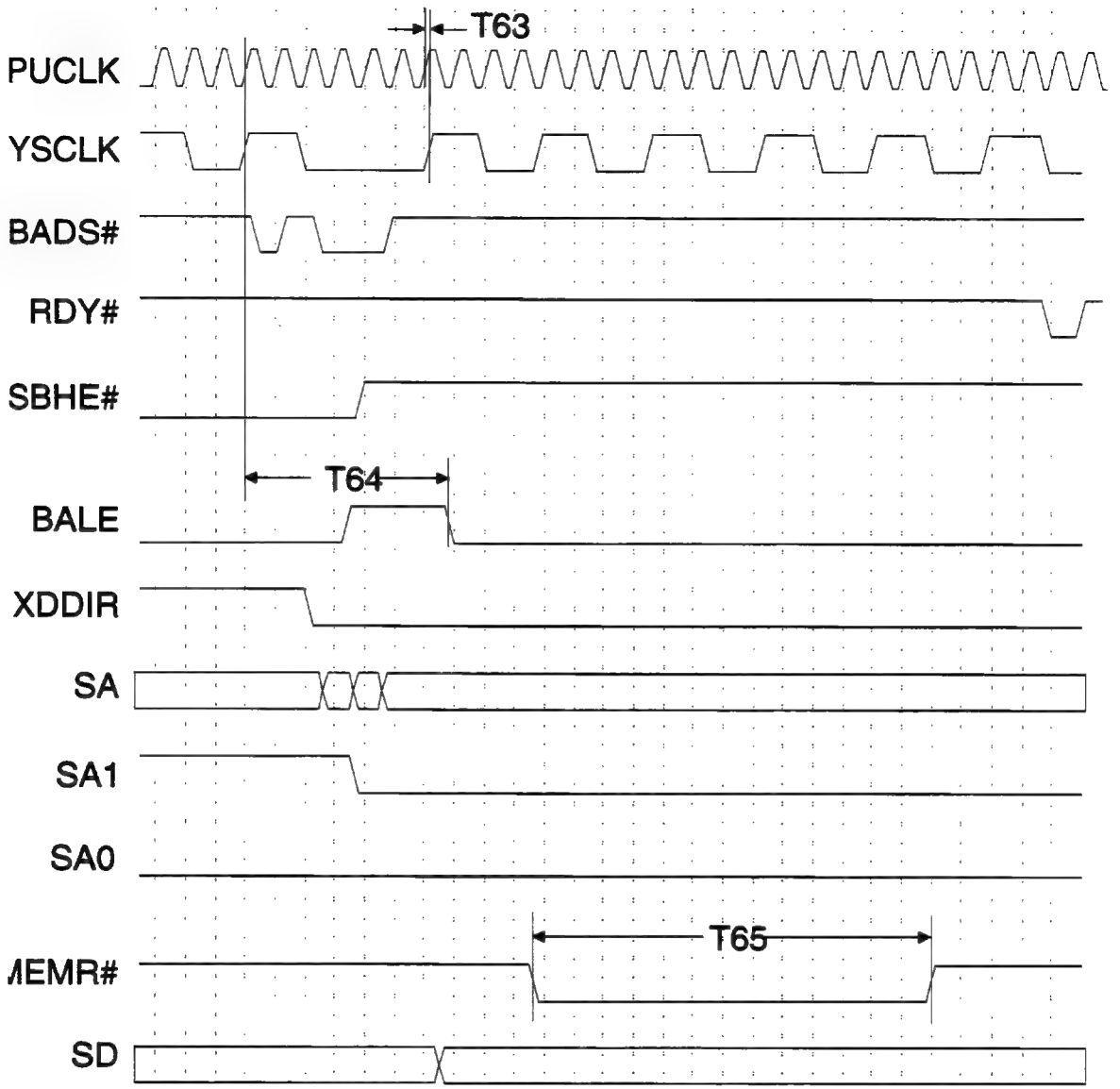
7.5.3 32-bit CPU Access to 16-bit AT Bus Memory Cycle



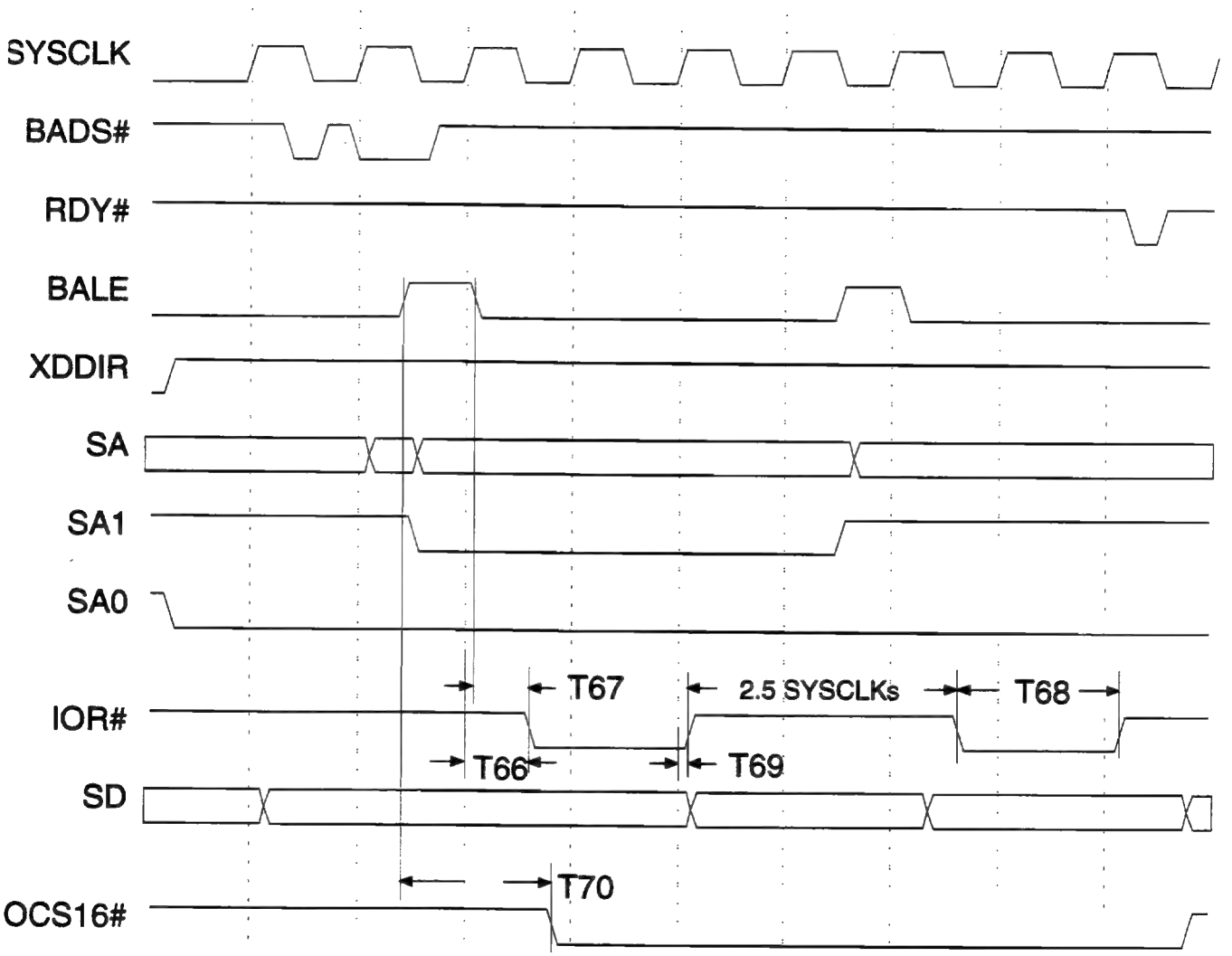
7.5.4 32-bit CPU Access to 8-bit AT Bus ROM Fetch Cycle



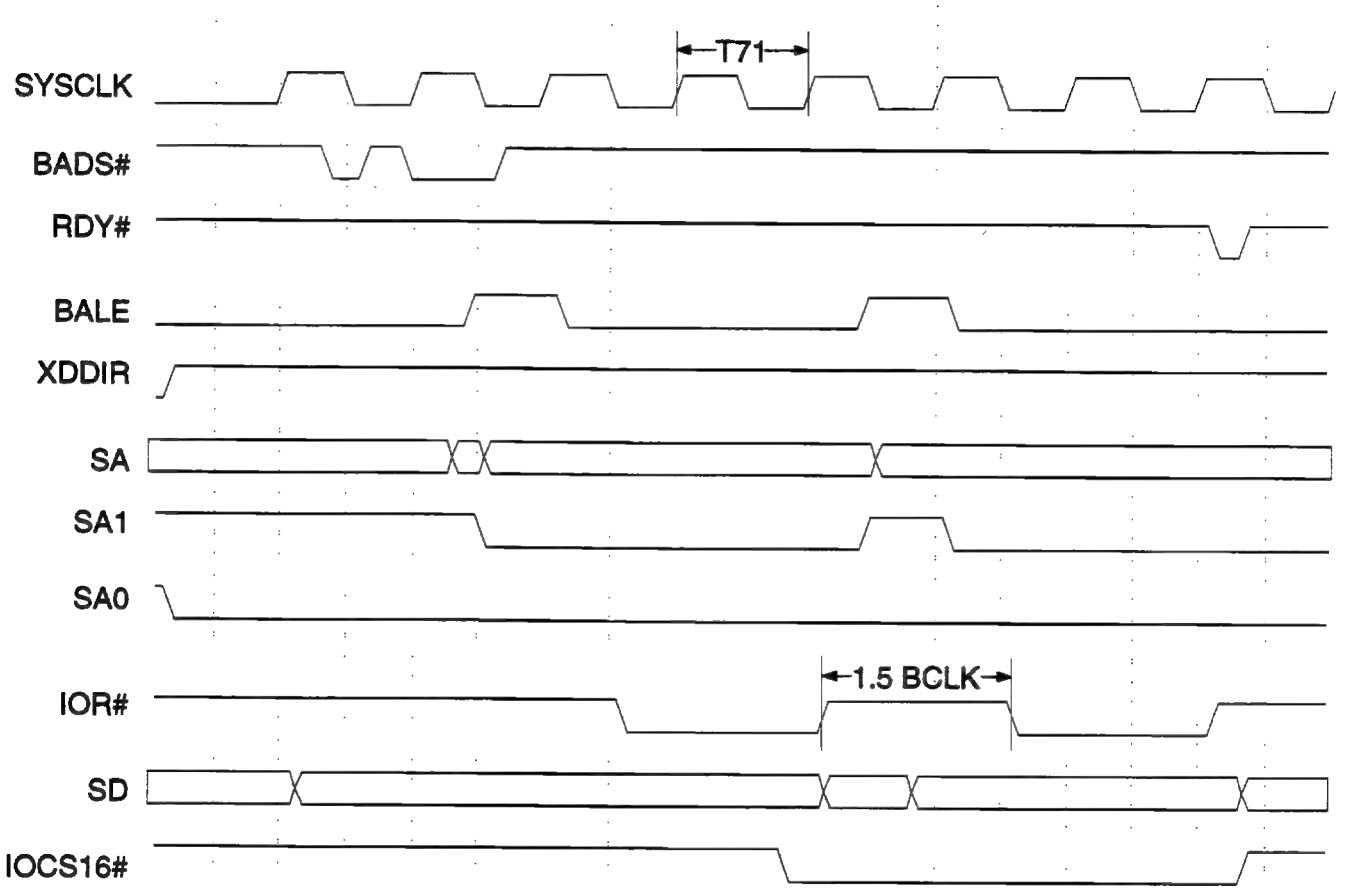
7.5.5 AT 8-bit Memory Read Cycle



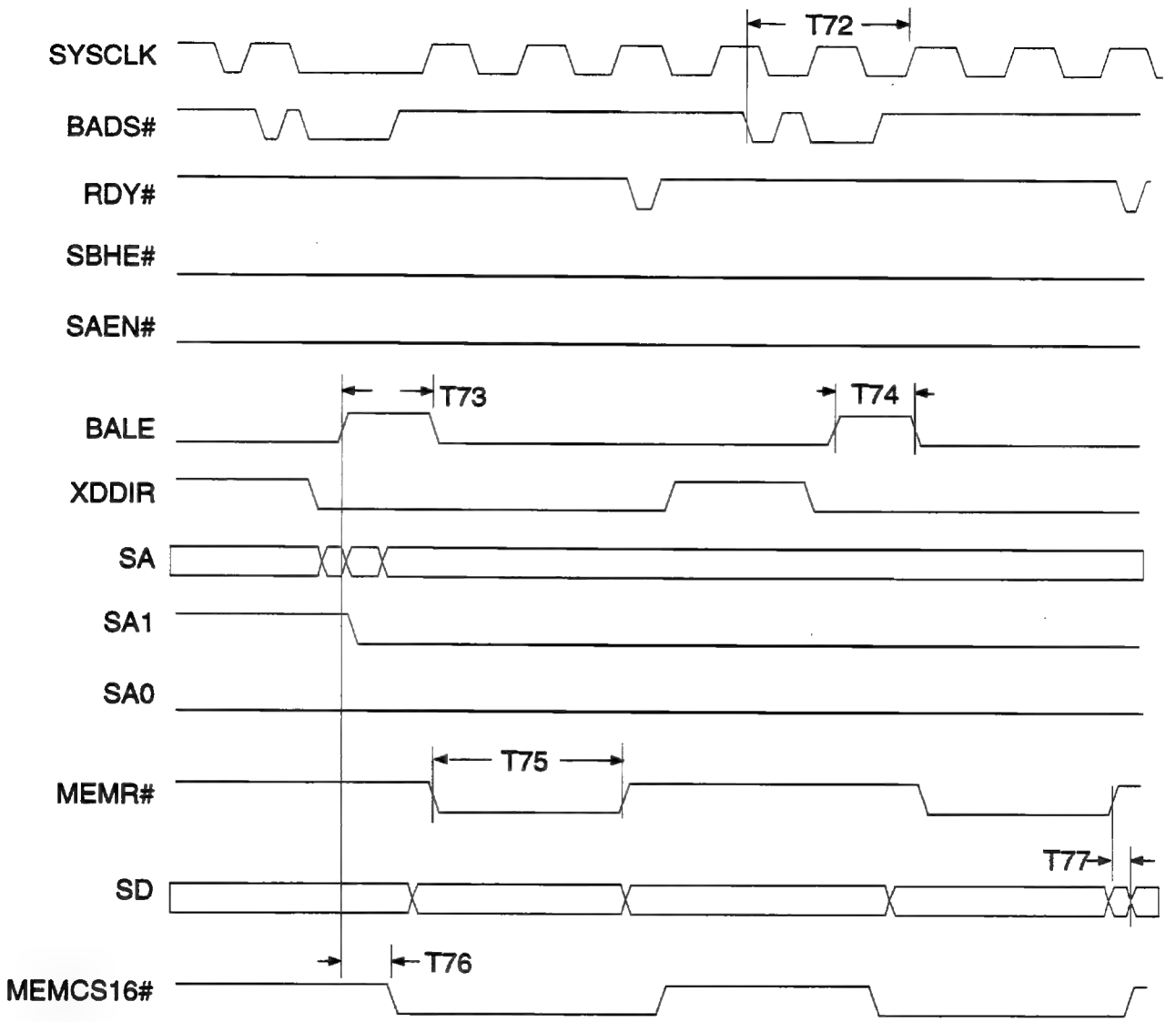
7.5.6 32-bit CPU Access to 16-bit AT Bus I/O Cycle with Back to Back Delay Optional:1



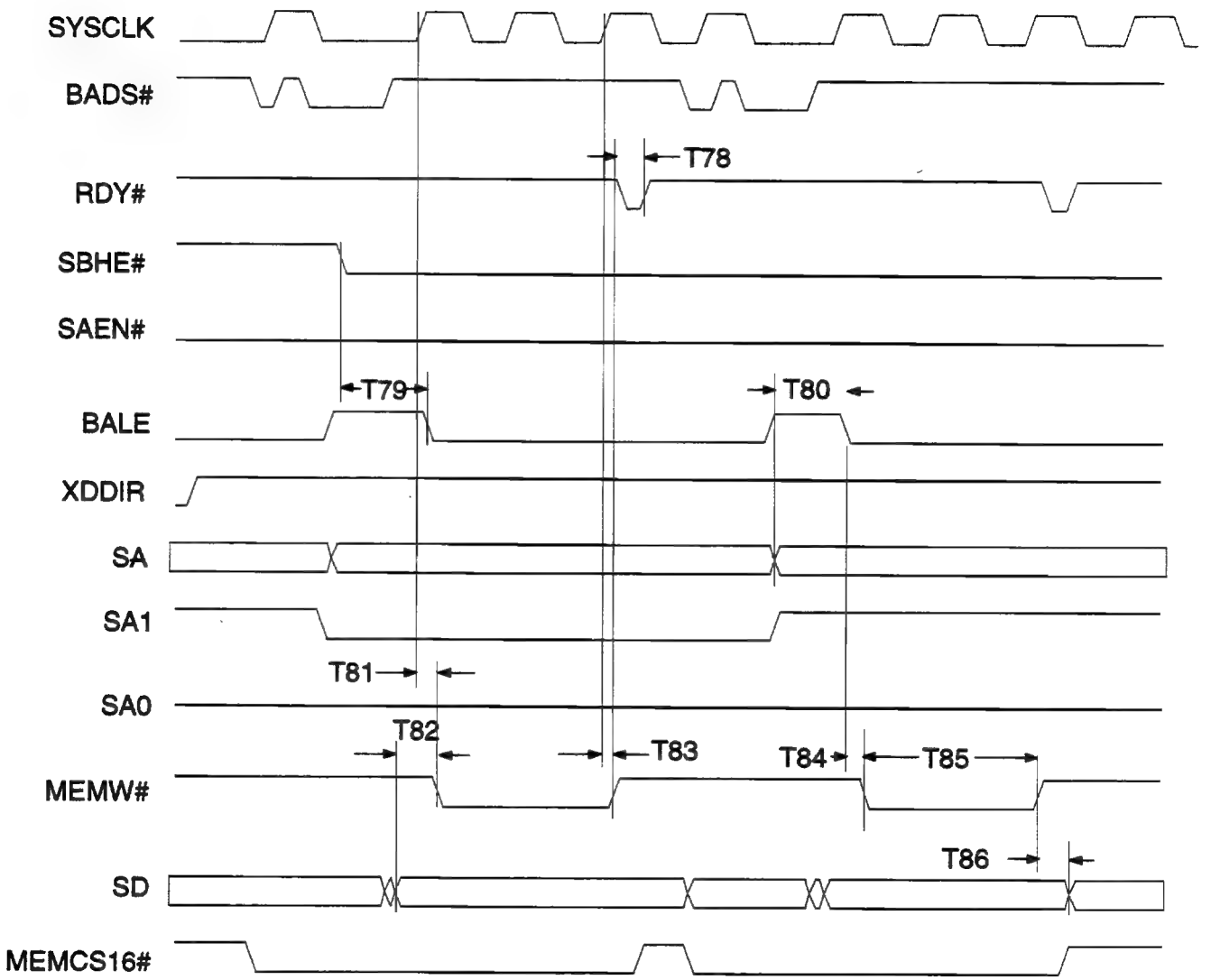
7.5.7 32-bit Access to 16-bit AT Bus I/O Cycle
with Back to Back Delay Optional: 0



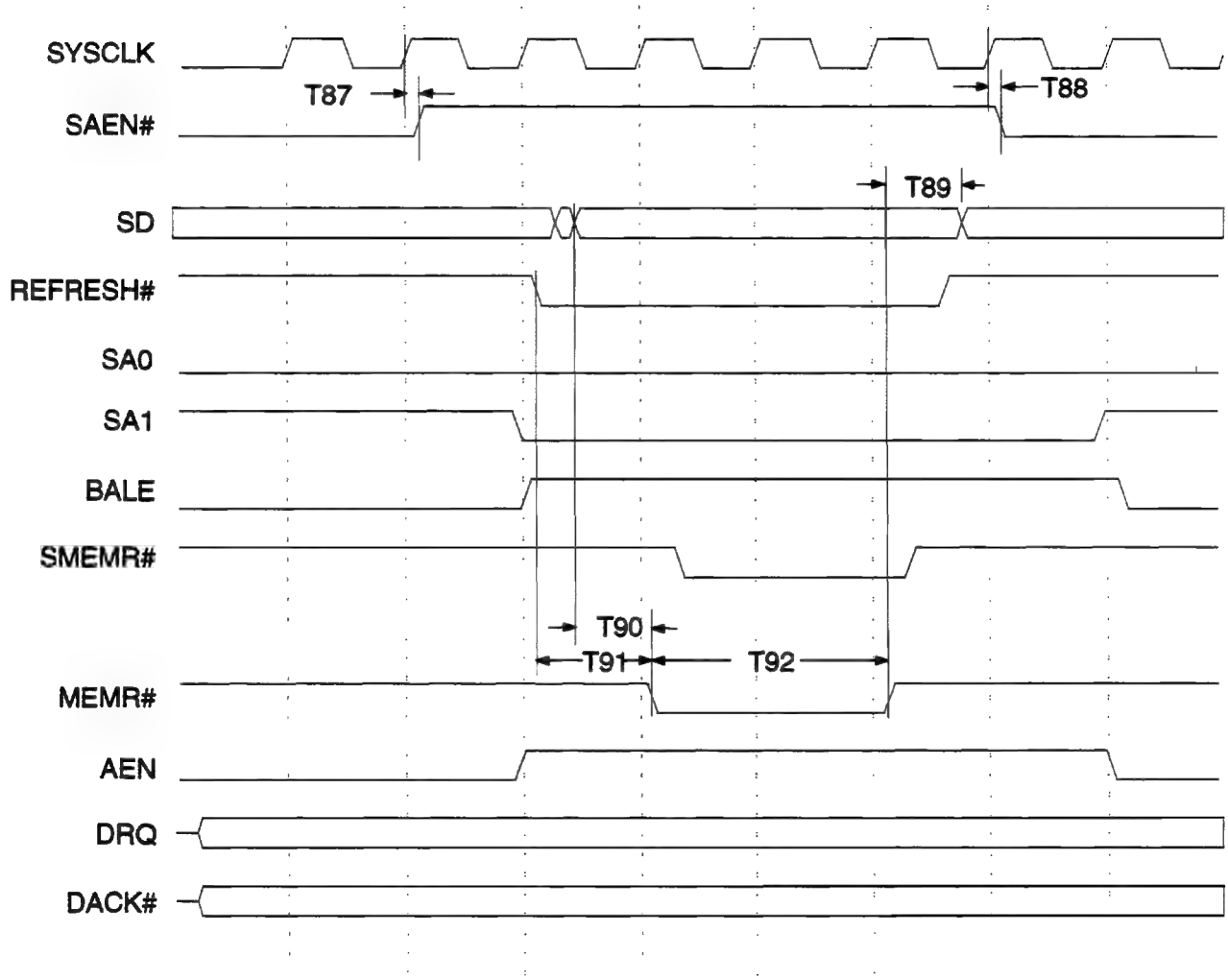
7.5.8 AT Bus 16-bit Memory Timing: 1WS



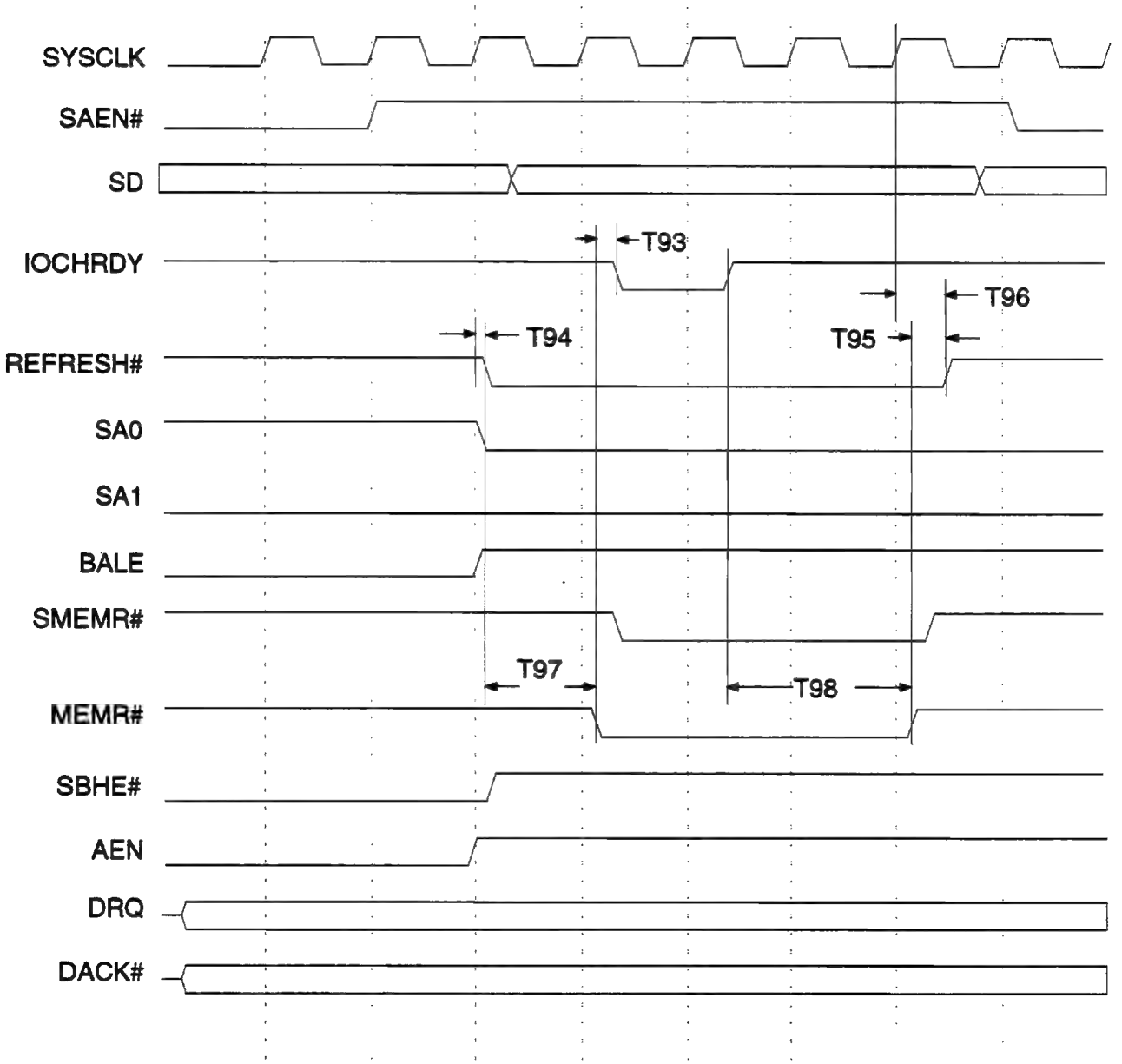
7.5.9 AT Bus 16-bit Memory Timing: 1WS



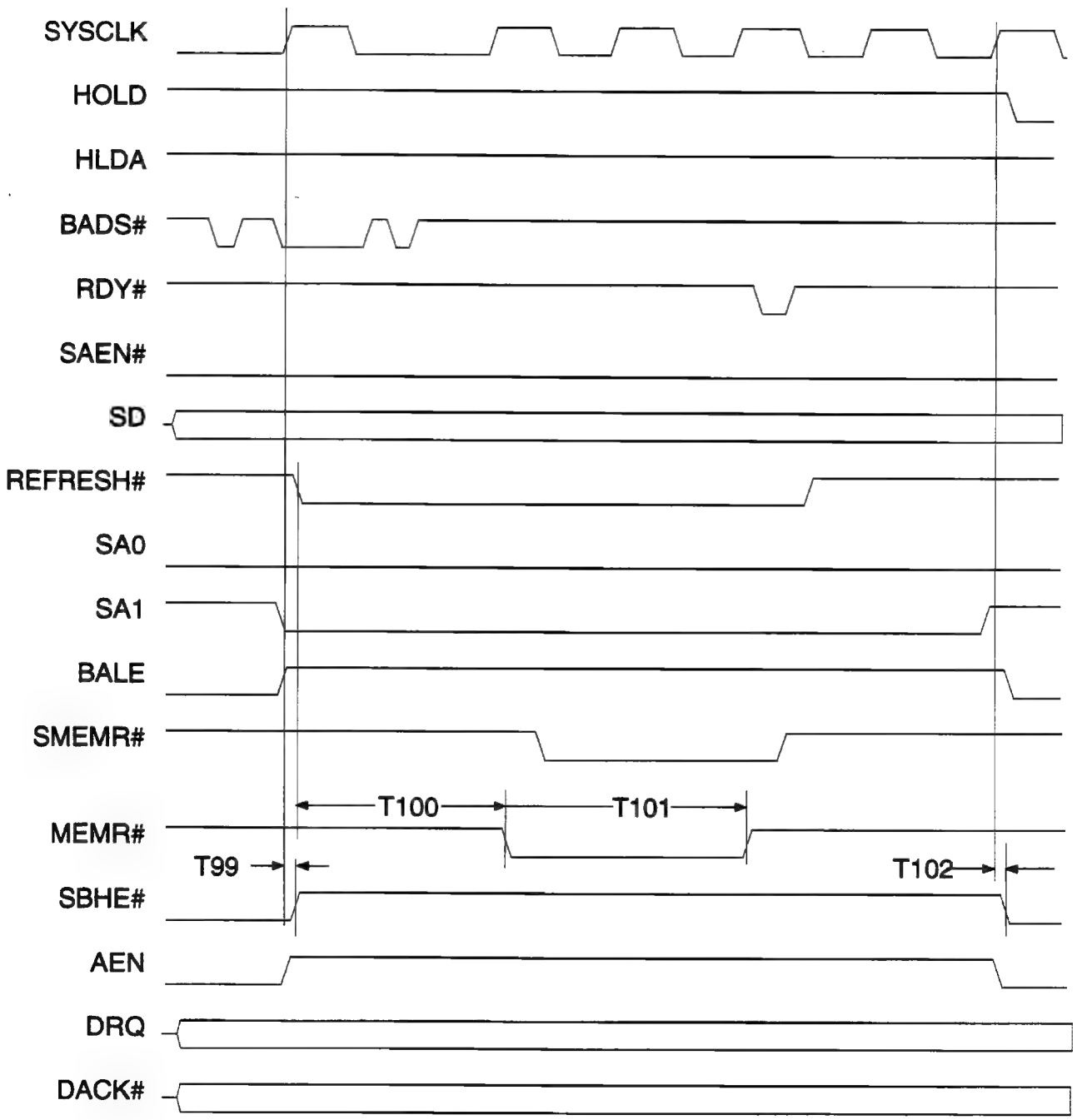
7.5.10 AT Hidden Refresh Cycle



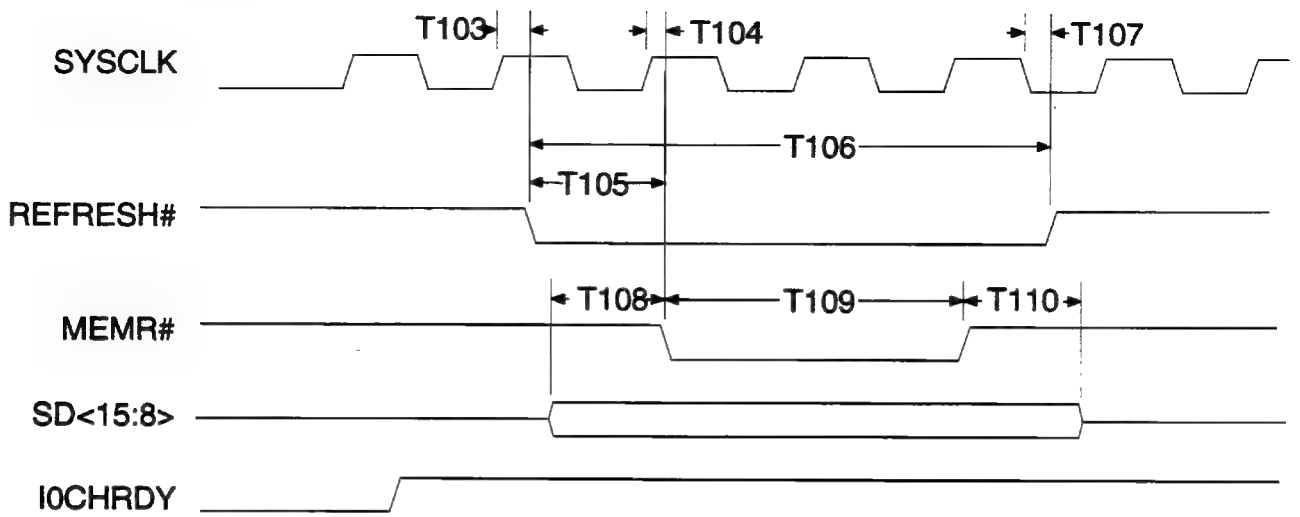
7.5.11 AT Hidden Refresh Cycle with IOCHRDY



7.5.12 AT Non-hidden Refresh Cycle

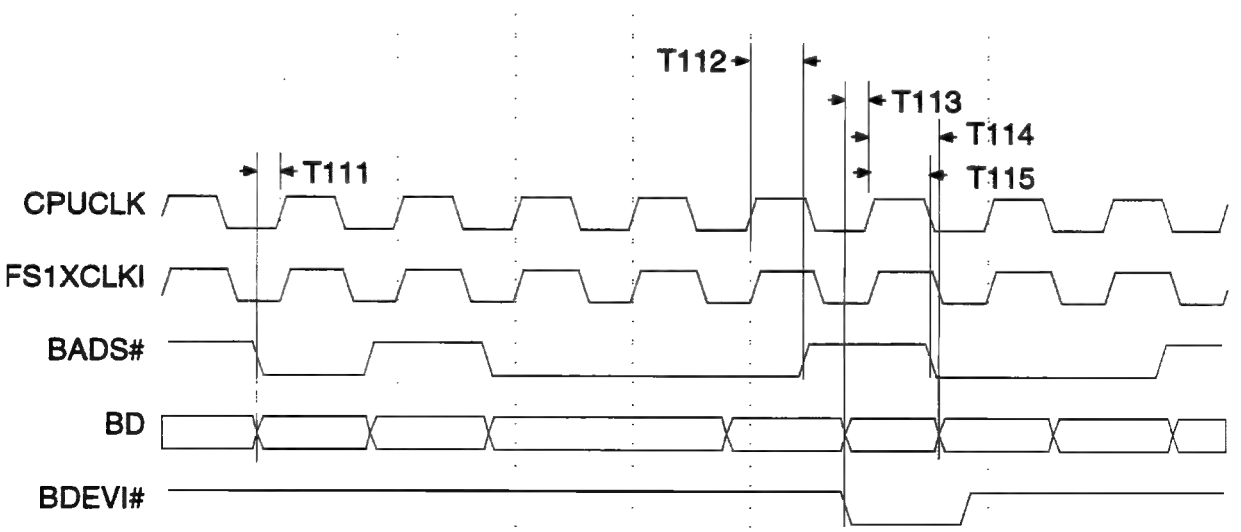


7.5.13 AT Refresh SYSCLK: Programmable

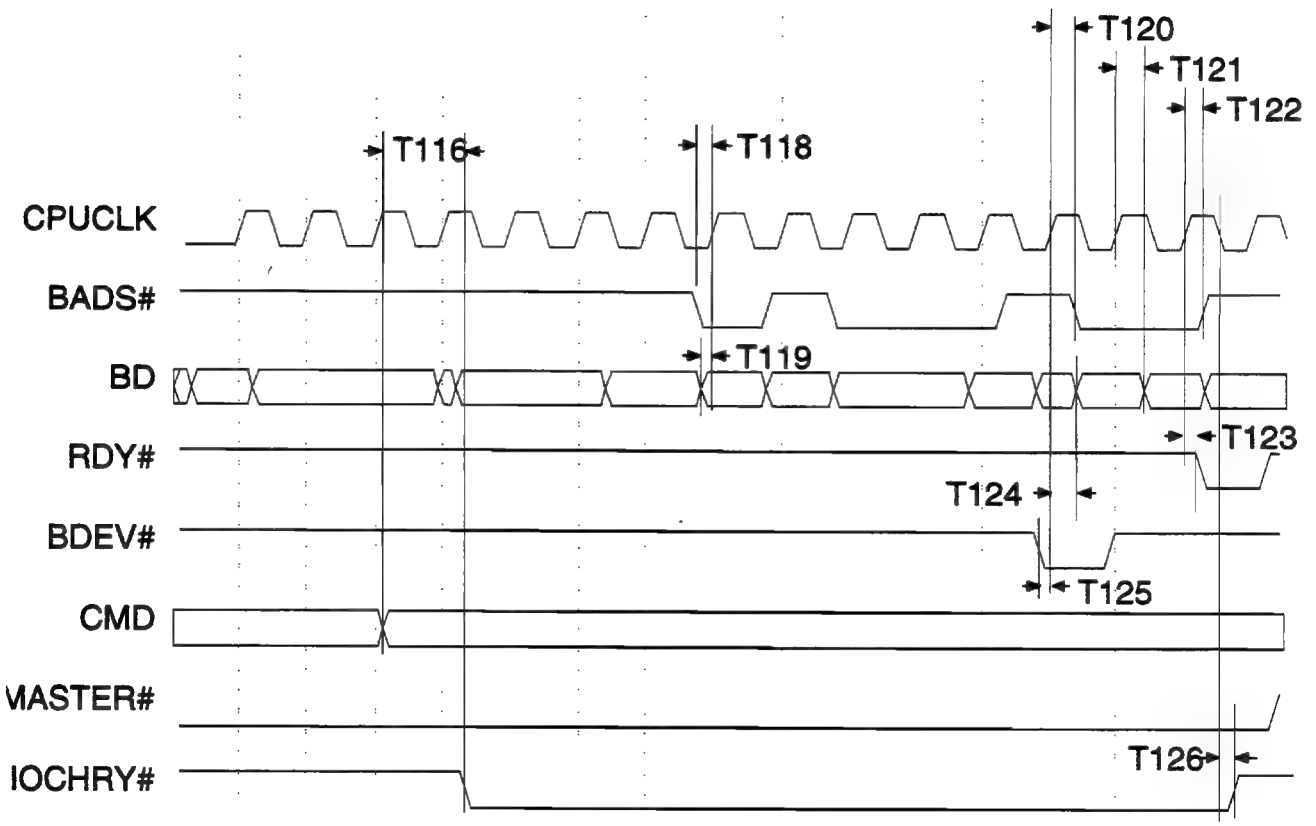


7.6 Burst Bus Interface

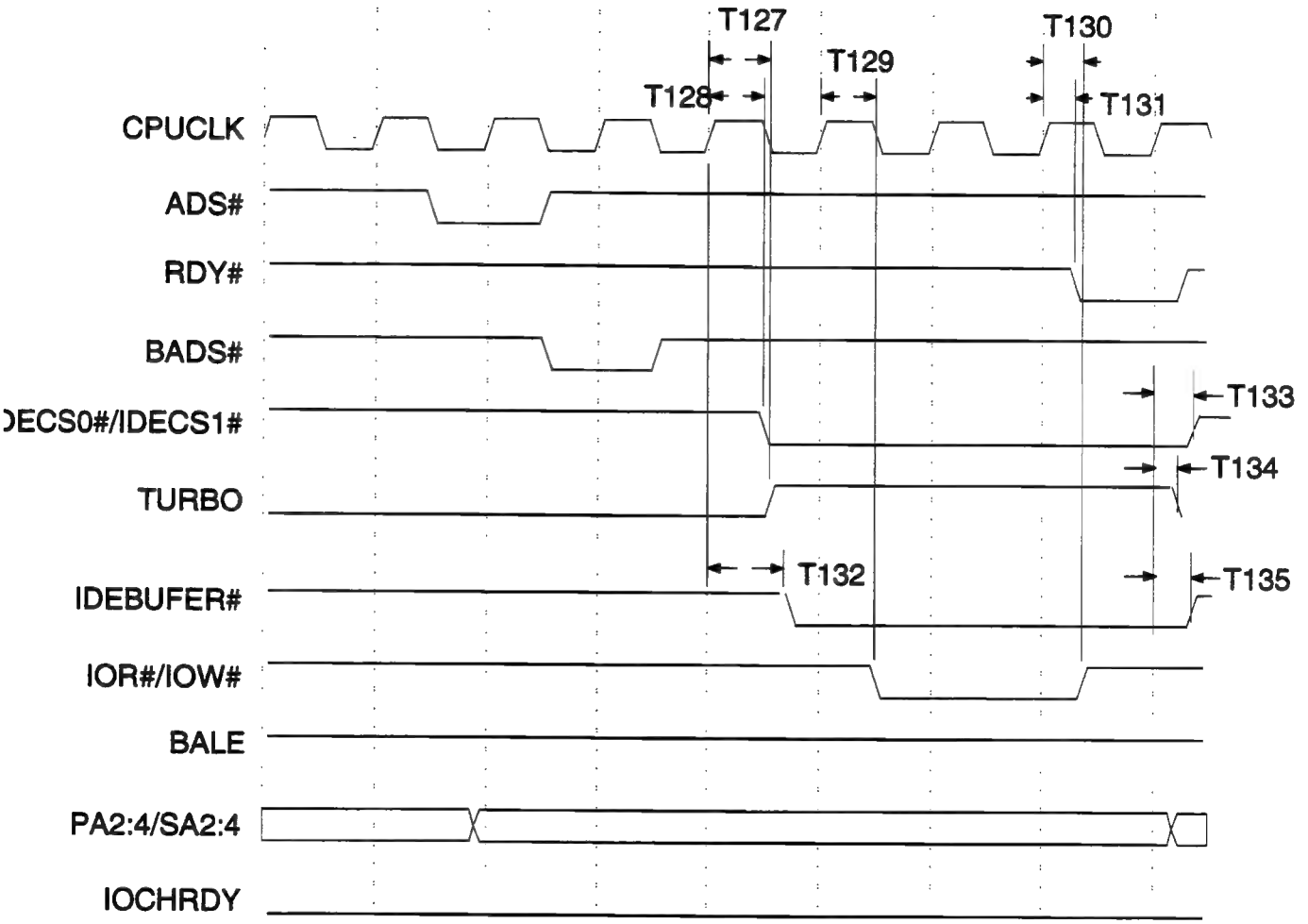
7.6.1 CPU Access Burst Bus Device



7.6.2 ISA Master Access Burst Bus



7.7 Local IDE Interface



8.0 Electrical Specifications

Note: All figures represent target characteristics. All parameters have not been fully characterized and are subject to change.

8.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITION	RATED VALUE	UNITS
Power Supply Voltage	VDD	Ta = 25°C	-0.5 to +6.5	V
Input Voltage	V_I		-0.5 to VDD +0.5	V
Output Voltage	V_O		-0.5 to VDD +0.5	V
Output Current Per I/O	I_O	VSS = 0V	TBD	mA
Current Per Power Pin	I_{PAD}		TBD	mA
Storage Temperature			-65 to +150	°C
ESD Voltage (Mil-Std-883C 3015.7)			4000	V
Input/Output Latch-up Current			± 200	mA

8.2 Operating Conditions (@5v core 33 Mhz)

PARAMETER	SYMBOL	*TARGET* RATED VALUE			UNITS
		MIN	TYP	MAX	
Power Supply Voltage	VDD	4.5	5.0	5.5	V
Power Supply Current (Redwood 1)	IDD		120		mA
Power Supply Current (Redwood 2)	IDD		80		mA
Temperature	T	0	25	70	°C

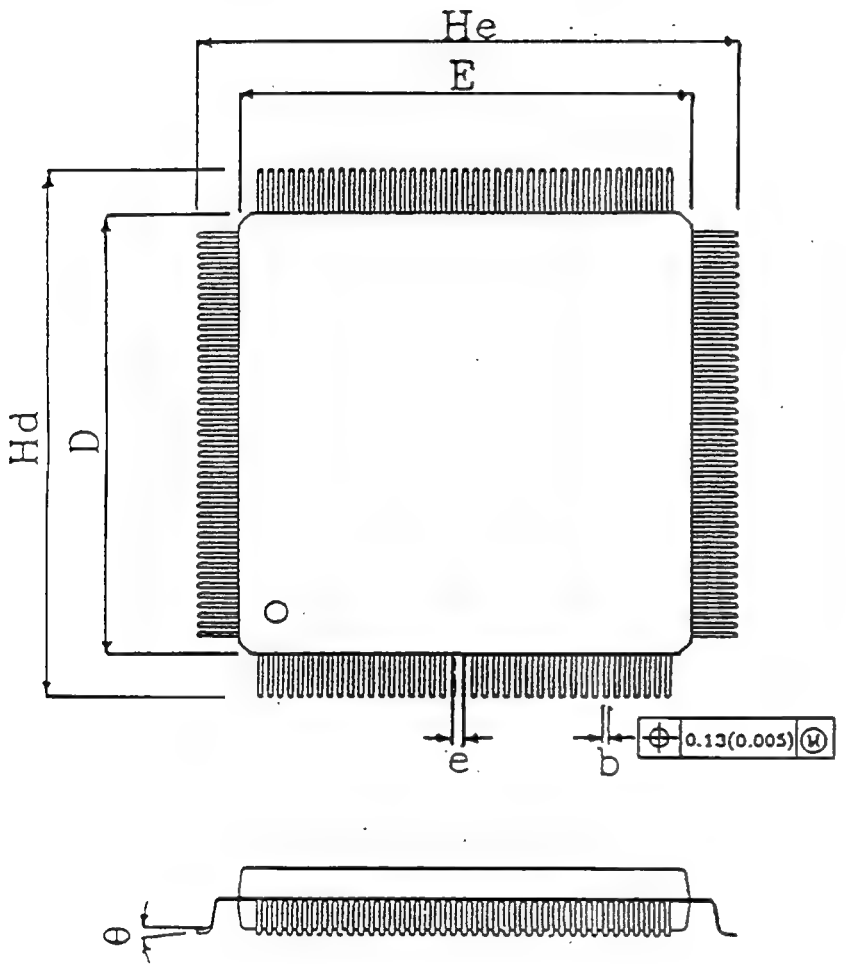
8.3 DC Characteristics

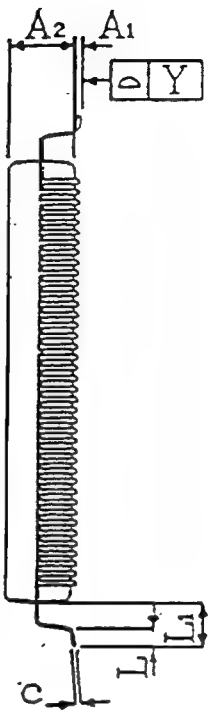
ITEM	SYM	CONDITION	SPECIFIED VALUE			UNIT
			MIN	TYP(1)	MAX	
High level input voltag	V_{IH}	TTL level input	2.2	—	V_{DD} + 0.5	V
		CMOS level input	0.7 V_{DD}	—	V_{DD} + 0.5	
Low level input voltage	V_{IL}	TTL level input	-0.5	—	0.8	V
		CMOS level input	-0.5	—	0.3 V_{DD}	
Schmitt trigger input threshold	V_{t+}	TTL level inputs	—	1.7	2.2	V
	V_{t-}		0.8	1.3	—	
	DVT	TTL Hysteresis (V_{t+} - V_{t-})	0.2	0.4	—	
	V_{t+}	CMOS level inputs	—	3.1	.76 V_{DD}	
	V_{t-}		0.24 V_{DD}	1.8	—	
	DVT	CMOS Hysteresis (V_{t+} - V_{t-})	0.6	1.3	—	
"H" level output voltage	V_{OH}	I_{OH} = 2,4,8,12 mA	3.7	—	—	V
"L" level output voltage	V_{OL}	I_{OL} = 2,4,8,12 mA	—	—	0.4	V
"H" level input current	I_{IH}	$V_{IH} = V_{DD}$	—	0.01	10	mA
"L" level input current	I_{IL}	$V_{IL} = V_{SS}$	-10	-0.01	—	mA
Tri-state output	I_{OZH}	$V_{OH} = V_{DD}$	—	0.01	10	mA
Leakage current	I_{OZL}	$V_{OL} = V_{SS}$	-10	0.01	—	
Stand-by current	I_{DDS}	Outputs open $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$	—	20	100	µA

Notes: (1) Typical condition is V_{DD} = 5.0V and T_a = 25°C

9.0 Package Specifications

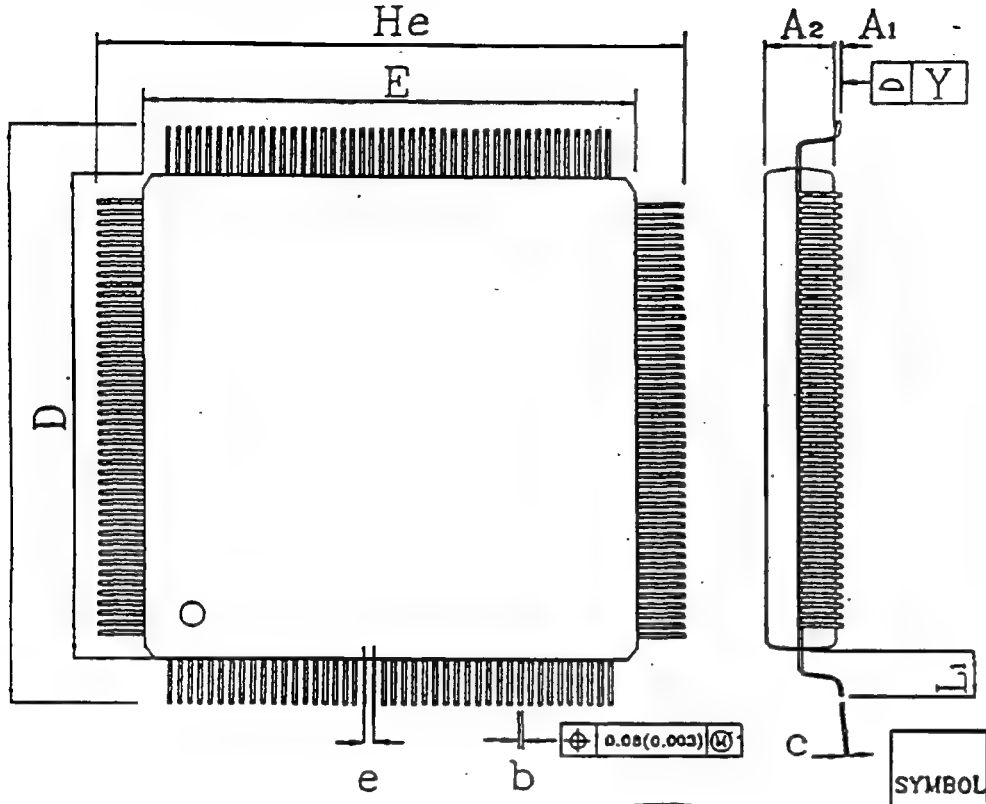
9.1 160-Pin PQFP Package Dimensions

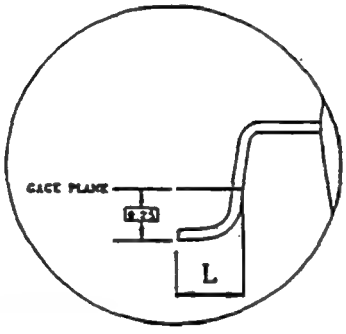


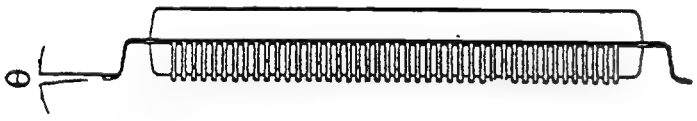


SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A_1	0.05	0.25	0.50	0.002	0.010	0.020
A_2	3.17	3.32	3.47	0.125	0.131	0.137
b	0.20	0.30	0.40	0.008	0.012	0.016
c	0.10	0.15	0.20	0.004	0.006	0.008
D	27.90	28.00	28.10	1.098	1.102	1.106
E	27.90	28.00	28.10	1.098	1.102	1.106
e		0.65			0.026	
Hd	30.95	31.20	31.45	1.218	1.228	1.238
He	30.95	31.20	31.45	1.218	1.228	1.238
L	0.65	0.80	0.95	0.025	0.031	0.037
L_1		1.60			0.063	
Y			0.08			0.003
θ	0		10	0		10

9.2 176-Pin TQFP Package Dimensions







SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A_1	0.05	0.10	0.15	0.002	0.004	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.090		0.200	0.004		0.008
D	23.90	24.00	24.10	0.941	0.945	0.949
E	23.90	24.00	24.10	0.941	0.945	0.949
e		0.50			0.020	
Hd	25.90	26.00	26.10	1.020	1.024	1.028
He	25.90	26.00	26.10	1.020	1.024	1.028
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1		1.00			0.039	
Y			0.08			0.003
θ	0		7	0		7

Appendix A - Summary of REDWOOD Registers

A.0 REDWOOD Configuration Registers

All REDWOOD configuration registers are indexed at address 24H and all data are accessed at address 26H. (There are the same addresses and accessing scheme as the previous three generations of EverGreen core logic controllers).

A.1 REDWOOD 1 Register Summary

The following is a summary of configuration registers for REDWOOD 1. For detailed register descriptions, refer to the appropriate section in the REDWOOD data book. The summary is listed by section number.

4.1 System Register Summary

4.1.0 Power-On Register	Configuration Index 100H
4.1.1 Non-Cacheable Region 1 Register	Configuration Index 101H
4.1.2 Non-Cacheable Region 2 Register	Configuration Index 102H
4.1.3 SYS Miscellaneous Control Register 1	Configuration Index 103H
4.1.4 SYS Miscellaneous Control Register 2	Configuration Index 104H
4.1.5 Parity Address Register 1	Configuration Index 105H
4.1.6 Parity Address Register 2	Configuration Index 106H
4.1.7 Shadow Register for Programmable Range 0/1	Configuration Index 080H
4.1.8 Shadow Register for Programmable Range 2/3	Configuration Index 081H
4.1.9 RTC Shadow Register	Configuration Index 086H
4.1.10 Modular Clock Control Register	Configuration Index 118H
4.1.11 Reserved	Configuration Index 180H

4.2 REDWOOD 1 Pin Function Select Registers

4.2.0 REDWOOD 1 Pin Select Register 1	Configuration Index 110H
4.2.1 REDWOOD 1 Pin Select Register 2	Configuration Index 111H
4.2.2 REDWOOD 1 Pin Select Register 3	Configuration Index 112H

4.3 DRAM Controller Register Summary

4.3.0 Shadow RAM Read Enable Control Register	Configuration Index 200H
4.3.1 Shadow RAM Write Enable Control Register	Configuration Index 201H
4.3.2 Bank 0 Control Register	Configuration Index 202H
4.3.3 Bank 1 Control Register	Configuration Index 203H
4.3.4 Bank 0/1 Timing Control Register	Configuration Index 204H
4.3.5 Bank 2 Control Register	Configuration Index 205H
4.3.6 Bank 3 Control Register	Configuration Index 206H

4.3.7 Bank 2/3 Timing Control Register	Configuration Index 207H
4.3.8 Bank 4 Control Register	Configuration Index 208H
4.3.9 Bank 5 Control Register	Configuration Index 209H
4.3.10 Bank 4/5 Timing Control Register	Configuration Index 20AH
4.3.11 DRAM Configuration Register 1	Configuration Index 20BH
4.3.12 DRAM Configuration Register 2	Configuration Index 20CH
4.3.13 DRAM Configuration Register 3	Configuration Index 20DH
4.3.14 DRAM Configuration Register 4	Configuration Index 20EH
4.3.15 DRAM Configuration Register 5	Configuration Index 20FH

4.4 Power Management Controller Register Summary

4.4.0 PMC Clock Control Register	Configuration Index 000H
4.4.1 Power Management Status Register	Configuration Index 001H
4.4.2 Activity Source Register	Configuration Index 002H
4.4.3 Primary Activity Mask Register	Configuration Index 003H
4.4.4 PMI Mask Register	Configuration Index 004H
4.4.5 Heat Regulator Control Register	Configuration Index 005H
4.4.6 PMI Mask and Control Register	Configuration Index 006H
4.4.7 General Purpose Control Register	Configuration Index 007H
4.4.8 Stop Clock Control Register	Configuration Index 008H
4.4.9 Fully-On Mode Power Control Register	Configuration Index 009H
4.4.10 Doze Mode Power Control Register	Configuration Index 00AH
4.4.11 Sleep Mode Power Control Register	Configuration Index 00BH
4.4.12 Suspend Mode Power Control Register	Configuration Index 00CH
4.4.13 Timer Register	Configuration Index 00DH
4.4.14 PMC Miscellaneous Control Register 1	Configuration Index 00EH
4.4.15 Reserved	Configuration Index 00FH
4.4.16 GP Counter/Timer Register	Configuration Index 010H
4.4.17 GP Timer Compare Register	Configuration Index 011H
4.4.18 Reserved	Configuration Index 012H
4.4.19 PMC Miscellaneous Control Register 2	Configuration Index 013H
4.4.20 Optional GPIO Control Register 2	Configuration Index 014H
4.4.21 Reserved	Configuration Index 015H
4.4.22 Reserved	Configuration Index 016H
4.4.23 Reserved	Configuration Index 017H
4.4.24 Reserved	Configuration Index 018H
4.4.25 Secondary Activity Mask Register	Configuration Index 019H
4.4.26 Additional Activity Source Register	Configuration Index 01AH

4.4.27 Additional Primary Activity Mask Register	Configuration Index 01BH
4.4.28 Additional Secondary Activity Control Register	Configuration Index 01CH
4.4.29 Additional PMI Mask Register	Configuration Index 01DH
4.4.30 Miscellaneous Control Register	Configuration Index 01EH
4.4.31 REDWOOD 1 Identification Register	Configuration Index 01FH
4.4.32 Programmable Range Compare Register 0	Configuration Index 020H
4.4.33 Programmable Range Compare Register 0	Configuration Index 021H
4.4.34 Programmable Range Compare Register 1	Configuration Index 022H
4.4.35 Programmable Range Compare Register 1	Configuration Index 023H
4.4.36 Programmable Range Compare Register 2	Configuration Index 024H
4.4.37 Programmable Range Compare Register 2	Configuration Index 025H
4.4.38 Programmable Range Compare Register 3	Configuration Index 026H
4.4.39 Programmable Range Compare Register 3	Configuration Index 027H
4.4.40 Programmable Timeout Timer Register 0	Configuration Index 028H
4.4.41 Programmable Timeout Timer Register 1	Configuration Index 029H
4.4.42 Programmable Timeout Timer Register 2	Configuration Index 02AH
4.4.43 Programmable Timeout Timer Register 3	Configuration Index 02BH
4.4.44 Programmable Timeout Timer Source Register 1	Configuration Index 02CH
4.4.45 Programmable Timeout Timer Source Register 2	Configuration Index 02DH
4.4.46 Programmable Timeout Timer Source Register 3	Configuration Index 02EH
4.4.47 Programmable Timeout Timer Source Register 4	Configuration Index 02FH

4.5 Cache Controller Summary

4.5.0 Cache Control Register 1	Configuration Index 400H
4.5.1 Cache Control Register 2	Configuration Index 401H
4.5.2 Cache Control Register 3	Configuration Index 402H
4.5.3 Cache Control Register 4	Configuration Index 403H
4.5.4 Cache Control Register 5	Configuration Index 404H

A.2 REDWOOD 2 Register Summary

The following is a summary of configuration registers for REDWOOD 2. For detailed register descriptions, refer to the appropriate section in the REDWOOD data book. The summary is listed by section number.

5.1 Bus Controller Register Summary

5.1.0 AT Miscellaneous Control Register 1	Configuration Index 300H
5.1.1 AT Miscellaneous Control Register 2	Configuration Index 301H
5.1.2 REDWOOD 2 Identification Register	Configuration Index 310H

5.2 REDWOOD 2 Pin Function Select Register

5.2.0 REDWOOD 2 Pin Select Register	Configuration Index 302H

5.3 Miscellaneous Peripheral Control Register Summary

5.3.0 Miscellaneous DMA Control Register 1	Configuration Index 330H
5.3.1 Miscellaneous DMA Control Register 2	Configuration Index 331H
5.3.2 Reserved	Configuration Index 340H
5.3.3 Reserved	Configuration Index 341H

5.4 Additional Power Management Register Summary

5.4.0 Modular Clock Control Register	Configuration Index 303H
5.4.1 Primary Activities IRQ Mask Register	Configuration Index 350H
5.4.2 PMI Trigger Source IRQ Active Register	Configuration Index 351H
5.4.3 PMI Trigger Source IRQ Mask Register	Configuration Index 352H
5.4.4 IRQ Secondary Activity Enable Register	Configuration Index 353H
5.4.5 Optional GPIO Control Register	Configuration Index 304H

5.5 Shadow Register Summary

5.5.0 8254 Counter 0 Shadow Register 1	Configuration Index 500H
5.5.1 8254 Counter 0 Shadow Register 2	Configuration Index 501H
5.5.2 8254 Counter 1 Shadow Register 1	Configuration Index 502H
5.5.3 8254 Counter 1 Shadow Register 2	Configuration Index 503H
5.5.4 8254 Counter 2 Shadow Register 1	Configuration Index 504H
5.5.5 8254 Counter 2 Shadow Register 2	Configuration Index 505H
5.5.6 8254 Counter 0 Shadow Register 3	Configuration Index 506H
5.5.7 8254 Counter 1 Shadow Register 3	Configuration Index 507H
5.5.8 8254 Counter 2 Shadow Register 3	Configuration Index 508H

5.5.9 8237 DMA Controller Shadow Register 1	Configuration Index 510H
5.5.10 8237 DMA Controller Shadow Register 2	Configuration Index 511H
5.5.11 8237 DMA Controller Shadow Register 3	Configuration Index 512H
5.5.12 8237 DMA Controller Shadow Register 4	Configuration Index 513H
5.5.13 8237 DMA Controller Shadow Register 5	Configuration Index 514H
5.5.14 8237 DMA Controller Shadow Register 6	Configuration Index 515H
5.5.15 8237 DMA Controller Shadow Register 7	Configuration Index 516H
5.5.16 8237 DMA Controller Shadow Register 8	Configuration Index 517H
5.5.17 8259 Interrupt Controller Shadow Register 1	Configuration Index 520H
5.5.18 8259 Interrupt Controller Shadow Register 2	Configuration Index 521H
5.5.19 8259 Interrupt Controller Shadow Register 3	Configuration Index 522H
5.5.20 8259 Interrupt Controller Shadow Register 4	Configuration Index 523H
5.5.21 8259 Interrupt Controller Shadow Register 5	Configuration Index 524H
5.5.22 8259 Interrupt Controller Shadow Register 6	Configuration Index 525H
5.5.23 8259 Interrupt Controller Shadow Register 7	Configuration Index 526H
5.5.24 8259 Interrupt Controller Shadow Register 8	Configuration Index 527H
5.5.25 8259 Interrupt Controller Shadow Register 9	Configuration Index 528H
5.5.26 8259 Interrupt Controller Shadow Register 10	Configuration Index 529H
5.5.27 8259 Interrupt Controller Shadow Register 11	Configuration Index 52AH
5.5.28 8259 Interrupt Controller Shadow Register 12	Configuration Index 52BH

Appendix B - REDWOOD 1 Pin List

B.0 160 PQFP Pin List (by Pin Number)

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	A27	41	SWTCH	81	reserved	121	TAGWE#
2	A26	42	VSS9	82	MDEN#	122	TAGD7(HIT#)
3	A25	43	VSS8	83	DRAMWE#	123	TAGD6(PC9)
4	A24	44	GPIO0	84	CAS3B#	124	TAGD5(PC8)
5	A23	45	GPIO1	85	CAS2B#	125	TAGD4(PC7)
6	VSS11	46	GPIO2	86	CAS1B#	126	VSS2
7	A22	47	GPIO3	87	CAS0B#	127	TAGD3(PC6)
8	A21	48	MASTER#	88	CAS3A#	128	TAGD2(PC5)
9	A20	49	PWRGOOD	89	VDDIO2	129	TAGD1(PC4)
10	A19	50	RCRST#	90	CAS2A#	130	TAGD0
11	A18	51	32KIN	91	CAS1A#	131	VDDIO5
12	A17	52	VDDIO3	92	CAS0A#	132	DIRTY(WAKE0)
13	A16	53	CLK1X2X	93	VSS4	133	DRTWE#(WAKE1)
14	VDDIO1	54	VSS7	94	RAS2#	134	VDDCL0
15	A15	55	PC0	95	RAS1#	135	LOCK#(CA13)
16	A14	56	PC1	96	RAS0#	136	HITM#
17	A13	57	PC2	97	MA11	137	WB/WT#
18	A12	58	PC3	98	MA10	138	CACHE#
19	A11	59	RSTDRV#	99	MA9	139	BRDY#
20	A10	60	KBRST#	100	MA8	140	VSS1
21	A9	61	SPNDNRST	101	MA7	141	ADS#
22	A8	62	KBCS#	102	VDDIO2	142	RDY#
23	A7	63	ROMCS#	103	MA6	143	W/R#
24	A6	64	IRQ8#	104	MA5	144	D/C#
25	VSS10	65	BD7	105	MA4	145	M/IO#
26	A5	66	BD6	106	MA3	146	BLAST#
27	A4	67	BD5	107	MA2	147	EADS#
28	A3	68	BD4	108	MA1	148	A20M#
29	A2	69	BD3	109	VSS3	149	HLDA
30	SRESET	70	BD2	110	MA0B	150	VDDIO1
31	SMIACT#	71	BD1	111	MA0A	151	CPUCLK O2
32	RSTCPU	72	BD0	112	CCS0#(LB)	152	VSS0
33	FLUSH#	73	VDDIO4	113	CCS1#(VLB)	153	CPUCLK O1
34	VDDIO1	74	FS1XCLK	114	CCS2#(ACPWR)	154	BE3#
35	SMI#	75	BADS#	115	CCS3#	155	BE2#
36	STPCLK#	76	BDEV#	116	VDDIO5	156	BE1#
37	VDDCL1	77	BSER	117	CA3A(CA3)	157	BE0#
38	KEN#	78	VSS6	118	CA3B(CA2)	158	A31
39	COE0#	79	VSS5	119	CWE0#	159	NMI(EXTACT0)
40	COE1#	80	reserved	120	CWE1#	160	SRAMCE#

B.1 160 PQFP Pin List (by Pin Name)

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
51	32KIN	157	BE0#	136	HITM#	31	SMIACT#
20	A10	156	BE1#	149	HLDA	61	SPNDNRST
19	A11	155	BE2#	64	IRQ8#	160	SRAMCE#
18	A12	154	BE3#	62	KBCS#	30	SRESET
17	A13	146	BLAST#	60	KBRST#	36	STPCLK#
16	A14	139	BRDY#	38	KEN#	41	SWTCH
15	A15	77	BSER	135	LOCK#(CA13)	130	TAGD0
13	A16	117	CA3A(CA3)	145	M/IO#	129	TAGD1(PC4)
12	A17	118	CA3B(CA2)	111	MA0A	128	TAGD2(PC5)
11	A18	138	CACHE#	110	MA0B	127	TAGD3(PC6)
10	A19	92	CAS0A#	108	MA1	125	TAGD4(PC7)
29	A2	87	CAS0B#	98	MA10	124	TAGD5(PC8)
9	A20	91	CAS1A#	97	MA11	123	TAGD6(PC9)
148	A20M#	86	CAS1B#	107	MA2	122	TAGD7(HIT#)
8	A21	90	CAS2A#	106	MA3	121	TAGWE#
7	A22	85	CAS2B#	105	MA4	134	VDDCL0
5	A23	88	CAS3A#	104	MA5	37	VDDCL1
4	A24	84	CAS3B#	103	MA6	14	VDDIO1
3	A25	112	CCS0#(LB)	101	MA7	34	VDDIO1
2	A26	113	CCS1#(VLB)	100	MA8	150	VDDIO1
1	A27	114	CCS2#(ACPWR)	99	MA9	89	VDDIO2
28	A3	115	CCS3#	48	MASTER#	102	VDDIO2
158	A31	53	CLK1X2X	82	MDEN#	52	VDDIO3
27	A4	39	COE0#	159	NMI(EXTACT0)	73	VDDIO4
26	A5	40	COE1#	55	PC0	116	VDDIO5
24	A6	153	CPUCLK O1	56	PC1	131	VDDIO5
23	A7	151	CPUCLK O2	57	PC2	152	VSS0
22	A8	119	CWE0#	58	PC3	140	VSS1
21	A9	120	CWE1#	49	PWRGOOD	25	VSS10
141	ADS#	144	D/C#	96	RAS0#	6	VSS11
75	BADS#	132	DIRTY(WAKE0)	95	RAS1#	126	VSS2
72	BD0	83	DRAMWE#	94	RAS2#	109	VSS3
71	BD1	133	DRTWE#(WAKE1)	50	RCRST#	93	VSS4
70	BD2	147	EADS#	142	RDY#	79	VSS5
69	BD3	33	FLUSH#	80	reserved	78	VSS6
68	BD4	74	FS1XCLK	81	reserved	54	VSS7
67	BD5	44	GPIO0	63	ROMCS#	43	VSS8
66	BD6	45	GPIO1	32	RSTCPU	42	VSS9
65	BD7	46	GPIO2	59	RSTDRV#	143	W/R#
76	BDEV#	47	GPIO3	35	SMI#	137	WB/WT#

B.2 176 TQFP Pin List (by Pin Number)

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	nc	45	nc	89	reserved	133	nc
2	nc	46	nc	90	reserved	134	nc
3	A27	47	SWTCH	91	reserved	135	TAGWE#
4	A26	48	VSSIO	92	MDEN#	136	TAGD7
5	A25	49	VSSIO	93	DRAMWE#	137	TAGD6
6	A24	50	GPIO0	94	CAS3B#	138	TAGD5
7	A23	51	GPIO1	95	CAS2B#	139	TAGD4
8	VSSIO	52	GPIO2	96	CAS1B#	140	VSSIO
9	A22	53	GPIO3	97	CAS0B#	141	TAGD3
10	A21	54	MASTER#	98	CAS3A#	142	TAGD2
11	A20	55	PWRGOOD	99	VCC	143	TAGD1
12	A19	56	RCRST#	100	CAS2A#	144	TAGD0
13	A18	57	32KIN	101	CAS1A#	145	VCC
14	A17	58	VCC	102	CAS0A#	146	DIRTY
15	A16	59	CLK1X2X	103	VSSIO	147	DRTWE#
16	VCC	60	VSSIO	104	RAS2#	148	VCC
17	A15	61	PC0	105	RAS1#	149	LOCK#
18	A14	62	PC1	106	RAS0#	150	HITM#
19	A13	63	PC2	107	MA11	151	WB/WT#
20	A12	64	PC3	108	MA10	152	CACHE#
21	A11	65	RSTDRV#	109	MA9	153	BRDY#
22	A10	66	KBRST#	110	MA8	154	VSSIO
23	A9	67	SPNDNRST	111	MA7	155	ADS#
24	A8	68	KBCS#	112	VCC	156	RDY#
25	A7	69	ROMCS#	113	MA6	157	W/R#
26	A6	70	IRQ8#	114	MA5	158	D/C#
27	VSSIO	71	BD7	115	MA4	159	M/IO#
28	A5	72	BD6	116	MA3	160	BLAST#
29	A4	73	BD5	117	MA2	161	EADS#
30	A3	74	BD4	118	MA1	162	A20M#
31	A2	75	BD3	119	VSSIO	163	HLDA
32	SRESET	76	BD2	120	MA0B	164	VCC
33	SMIACT#	77	BD1	121	MA0A	165	CPUCLK 02
34	RSTCPU	78	BD0	122	CCS0#	166	VSSIO
35	FLUSH#	79	VCC	123	CCS1#	167	CPUCLK 01
36	VCC	80	FS1XCLK	124	CCS2#	168	BE3#
37	SMI#	81	BADS#	125	CCS3#	169	BE2#
38	STPCLK#	82	BDEV#	126	VCC	170	BE1#
39	VCC	83	BSER	127	CA3A	171	BE0#
40	KEN#	84	VSSIO	128	CA3B	172	A31
41	COE0#	85	VSSIO	129	CWE0#	173	NMI
42	COE1#	86	reserved	130	CWE1#	174	SRAMCE#
43	nc	87	reserved	131	nc	175	nc
44	nc	88	reserved	132	nc	176	nc

B.3 176 TQFP Pin List (by Pin Name)

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
57	32KIN	160	BLAST#	50	GPIO0	55	PWRGOOD
22	A10	153	BRDY#	51	GPIO1	106	RAS0#
21	A11	83	BSER	52	GPIO2	105	RAS1#
20	A12	127	CA3A	53	GPIO3	104	RAS2#
19	A13	128	CA3B	150	HITM#	56	RCRST#
18	A14	152	CACHE#	163	HLDA	156	RDY#
17	A15	102	CAS0A#	70	IRQ8#	86	reserved
15	A16	97	CAS0B#	68	KBCS#	87	reserved
14	A17	101	CAS1A#	66	KBRST#	88	reserved
13	A18	96	CAS1B#	40	KEN#	89	reserved
12	A19	100	CAS2A#	149	LOCK#	90	reserved
31	A2	95	CAS2B#	121	MA0A	91	reserved
11	A20	98	CAS3A#	120	MA0B	69	ROMCS#
162	A20M#	94	CAS3B#	118	MA1	34	RSTCPU
10	A21	122	CCS0#	108	MA10	65	RSTDRV#
9	A22	123	CCS1#	107	MA11	37	SMI#
7	A23	124	CCS2#	117	MA2	33	SMIACT#
6	A24	125	CCS3#	116	MA3	67	SPNDNRST
5	A25	59	CLK1X2X	115	MA4	174	SRAMCE#
4	A26	41	COE0#	114	MA5	32	SRESET
3	A27	42	COE1#	113	MA6	38	STPCLK#
30	A3	167	CPUCLK 01	111	MA7	47	SWTCH
172	A31	165	CPUCLK 02	110	MA8	144	TAGD0
29	A4	129	CWE0#	109	MA9	143	TAGD1
28	A5	130	CWE1#	54	MASTER#	142	TAGD2
26	A6	158	D/C#	92	MDEN#	141	TAGD3
25	A7	146	DIRTY	159	M/IO#	139	TAGD4
24	A8	93	DRAMWE#	1	nc	138	TAGD5
23	A9	147	DRTWE#	2	nc	137	TAGD6
155	ADS#	161	EADS#	43	nc	136	TAGD7
81	BADS#	35	FLUSH#	44	nc	135	TAGWE#
78	BD0	80	FS1XCLK	45	nc	16	VCC
77	BD1	8	VSSIO	46	nc	36	VCC
76	BD2	27	VSSIO	131	nc	39	VCC
75	BD3	48	VSSIO	132	nc	58	VCC
74	BD4	49	VSSIO	133	nc	79	VCC
73	BD5	60	VSSIO	134	nc	99	VCC
72	BD6	84	VSSIO	175	nc	112	VCC
71	BD7	85	VSSIO	176	nc	126	VCC
82	BDEV#	103	VSSIO	173	NMI	145	VCC
171	BE0#	119	VSSIO	61	PC0	148	VCC
170	BE1#	140	VSSIO	62	PC1	164	VCC
169	BE2#	154	VSSIO	63	PC2	151	WB/WT#
168	BE3#	166	VSSIO	64	PC3	157	W/R#

Appendix C - REDWOOD 2 Pin List

C.0 160 PQFP Pin List (by Pin Number)

PIN#	NAME	PIN#	NAME	PIN#	NAME	PIN#	NAME
1	LREQ0#	41	VDDIO3	81	DACK6#	121	IDED7
2	LGNT0#	42	SMEMW#	82	DACK7#	122	IDEBUFEN#
3	D0	43	SMEMR#	83	VSS3	123	14MHZIN
4	D1	44	IOW#	84	IRQ1	124	VDDCL0
5	D2	45	IOR#	85	IRQ3	125	SPKR
6	VSS9	46	VSS7	86	IRQ4	126	DETURBO
7	D3	47	SD0	87	IRQ5	127	BSER
8	D4	48	SD1	88	IRQ6	128	reserved
9	D5	49	SD2	89	IRQ7	129	BDEV#
10	D6	50	SD3	90	IRQ8#	130	BADS#
11	VDDIO1	51	SD4	91	IRQ9	131	VSS1
12	D7	52	VSS6	92	IRQ10	132	FS1XCLK
13	D8	53	SD5	93	VDDIO3	133	VDDIO4
14	D9	54	SD6	94	IRQ11	134	BD7
15	D10	55	SD7	95	IRQ12	135	BD6
16	D11	56	SD8(MSA0)	96	IRQ14	136	BD5
17	D12	57	SD9(MSA1)	97	IRQ15	137	BD4
18	D13	58	SD10(MSA2)	98	SA0	138	BD3
19	D14	59	SD11(MSA3)	99	SA1	139	BD2
20	D15	60	SD12(MSA4)	100	SBHE#	140	BD1
21	D16	61	SD13(MSA5)	101	MEMCS16#	141	BD0
22	VSS8	62	SD14(MSA6)	102	VSS2	142	VSS0
23	D17	63	VSS5	103	MEMR#	143	CPUCLK
24	D18	64	SD15(MSA7)	104	MEMW#	144	LOCAL#
25	D19	65	DRQ0	105	AEN	145	HITM#(IRQ13)
26	D20	66	DACK0#	106	MASTER #	146	NMI
27	D21	67	DRQ1	107	IOCHCK#	147	HLDA
28	D22	68	VDDIO3	108	IOCHRDY	148	HOLD
29	D23	69	DACK1#	109	RSTDRV#	149	INTR
30	D24	70	DRQ2	110	ZWS#	150	reserved
31	D25	71	DACK2#	111	REFRESH#	151	IGNNE#
32	D26	72	VDDCL1	112	SYSCLK	152	FERR#
33	VDDIO1	73	DRQ3	113	BALE	153	DP3(GPIO7)
34	D27	74	DRQ5	114	IOCS16#	154	DP2(GPIO6)
35	D28	75	VSS4	115	VDDIO3	155	DP1(GPIO5)
36	D29	76	DRQ6	116	TURBO	156	DP0(GPIO4)
37	D30	77	DRQ7	117	SAEN#	157	BRDY#
38	D31	78	TC	118	reserved	158	RDY#
39	LRDY#	79	DACK3#	119	IDECS0#	159	LREQ1#
40	XDDIR	80	DACK5#	120	IDECS1#	160	LGNT1#

C.1 160 PQFP Pin List (by Pin Name)

PIN#	NAME	PIN#	NAME	PIN#	NAME	PIN#	NAME
123	14MHZIN	37	D30	114	IOCS16#	59	SD11(MSA3)
105	AEN	38	D31	45	IOR#	60	SD12(MSA4)
130	BADS#	8	D4	44	IOW#	61	SD13(MSA5)
113	BALE	9	D5	84	IRQ1	62	SD14(MSA6)
141	BD0	10	D6	92	IRQ10	64	SD15(MSA7)
140	BD1	12	D7	94	IRQ11	49	SD2
139	BD2	13	D8	95	IRQ12	50	SD3
138	BD3	14	D9	96	IRQ14	51	SD4
137	BD4	66	DACK0#	97	IRQ15	53	SD5
136	BD5	69	DACK1#	85	IRQ3	54	SD6
135	BD6	71	DACK2#	86	IRQ4	55	SD7
134	BD7	79	DACK3#	87	IRQ5	56	SD8(MSA0)
129	BDEV#	80	DACK5#	88	IRQ6	57	SD9(MSA1)
157	BRDY#	81	DACK6#	89	IRQ7	43	SMEMR#
127	BSER	82	DACK7#	90	IRQ8#	42	SMEMW#
143	CPUCLK	126	DETURBO	91	IRQ9	125	SPKR
3	D0	156	DP0(GPIO4)	2	LGNT0#	112	SYSCLK
4	D1	155	DP1(GPIO5)	160	LGNT1#	78	TC
15	D10	154	DP2(GPIO6)	144	LOCAL#	116	TURBO
16	D11	153	DP3(GPIO7)	39	LRDY#	124	VDDCL0
17	D12	65	DRQ0	1	LREQ0#	72	VDDCL1
18	D13	67	DRQ1	159	LREQ1#	11	VDDIO1
19	D14	70	DRQ2	106	MASTER #	33	VDDIO1
20	D15	73	DRQ3	101	MEMCS16#	41	VDDIO3
21	D16	74	DRQ5	103	MEMR#	68	VDDIO3
23	D17	76	DRQ6	104	MEMW#	93	VDDIO3
24	D18	77	DRQ7	146	NMI	115	VDDIO3
25	D19	152	FERR#	158	RDY#	133	VDDIO4
5	D2	132	FS1XCLK	111	REFRESH#	142	VSS0
26	D20	145	HITM#(IRQ13)	118	reserved	131	VSS1
27	D21	147	HLDA	128	reserved	102	VSS2
28	D22	148	HOLD	150	reserved	83	VSS3
29	D23	122	IDEBUFEN#	109	RSTDRV#	75	VSS4
30	D24	119	IDECS0#	98	SA0	63	VSS5
31	D25	120	IDECS1#	99	SA1	52	VSS6
32	D26	121	IDED7	117	SAEN#	46	VSS7
34	D27	151	IGNNE#	100	SBHE#	22	VSS8
35	D28	149	INTR	47	SD0	6	VSS9
36	D29	107	IOCHCK#	48	SD1	40	XDDIR
7	D3	108	IOCHRDY	58	SD10(MSA2)	110	ZWS#

C.2 176 TQFP Pin List (by Pin Number)

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	nc	45	nc	89	nc	133	nc
2	nc	46	nc	90	nc	134	nc
3	LREQ0#	47	VCC	91	DACK6#	135	IDED7
4	LGNT0#	48	SMEMW#	92	DACK7#	136	IDEBUFEN#
5	D0	49	SMEMR#	93	GND	137	14MHZIN
6	D1	50	IOW#	94	IRQ1	138	VCC
7	D2	51	IOR#	95	IRQ3	139	SPKR
8	GND	52	GND	96	IRQ4	140	DETURBO
9	D3	53	SD0	97	IRQ5	141	BSER
10	D4	54	SD1	98	IRQ6	142	BINT#
11	D5	55	SD2	99	IRQ7	143	BDEV#
12	D6	56	SD3	100	IRQ8#	144	BADS#
13	VCC	57	SD4	101	IRQ9	145	GND
14	D7	58	GND	102	IRQ10	146	FS1XCLK
15	D8	59	SD5	103	VCC	147	VCC
16	D9	60	SD6	104	IRQ11	148	BD7
17	D10	61	SD7	105	IRQ12	149	BD6
18	D11	62	SD8	106	IRQ14	150	BD5
19	D12	63	SD9	107	IRQ15	151	BD4
20	D13	64	SD10	108	SA0	152	BD3
21	D14	65	SD11	109	SA1	153	BD2
22	D15	66	SD12	110	SBHE#	154	BD1
23	D16	67	SD13	111	MEMCS16#	155	BD0
24	GND	68	SD14	112	GND	156	GND
25	D17	69	GND	113	MEMR#	157	CPUCLK
26	D18	70	SD15	114	MEMW#	158	LOCAL#
27	D19	71	DRQ0	115	AEN	159	HITM#
28	D20	72	DACK0#	116	MASTER#	160	NMI
29	D21	73	DRQ1	117	IOCHCK#	161	HLDA
30	D22	74	VCC	118	IOCHRDY	162	HOLD
31	D23	75	DACK1#	119	RSTDRV#	163	INTR
32	D24	76	DRQ2	120	ZWS#	164	reserved
33	D25	77	DACK2#	121	REFRESH#	165	IGNNE#
34	D26	78	VCC	122	SYSCLK	166	FERR#
35	VCC	79	DRQ3	123	BALE	167	DP3
36	D27	80	DRQ5	124	IOCS16#	168	DP2
37	D28	81	GND	125	VCC	169	DP1
38	D29	82	DRQ6	126	TURBO	170	DP0
39	D30	83	DRQ7	127	SAEN#	171	BRDY#
40	D31	84	TC	128	reserved	172	RDY#
41	LRDY#	85	DACK3#	129	IDECS0#	173	LREQ1#
42	XDDIR	86	DACK5#	130	IDECS1#	174	LGNT1#
43	nc	87	nc	131	nc	175	nc
44	nc	88	nc	132	nc	176	nc

C.3 176 TQFP Pin List (by Pin Name)

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
137	14MHZIN	11	D5	163	INTR	176	nc
115	AEN	12	D6	117	IOCHCK#	160	NMI
144	BADS#	14	D7	118	IOCHRDY	172	RDY#
123	BALE	15	D8	124	IOCS16#	121	REFRESH#
155	BD0	16	D9	51	IOR#	128	reserved
154	BD1	72	DACK0#	50	IOW#	164	reserved
153	BD2	75	DACK1#	94	IRQ1	119	RSTDRV#
152	BD3	77	DACK2#	102	IRQ10	108	SA0
151	BD4	85	DACK3#	104	IRQ11	109	SA1
150	BD5	86	DACK5#	105	IRQ12	127	SAEN#
149	BD6	91	DACK6#	106	IRQ14	110	SBHE#
148	BD7	92	DACK7#	107	IRQ15	53	SD0
143	BDEV#	140	DETURBO	95	IRQ3	54	SD1
142	BINT#	170	DP0	96	IRQ4	64	SD10
171	BRDY#	169	DP1	97	IRQ5	65	SD11
141	BSER	168	DP2	98	IRQ6	66	SD12
157	CPUCLK	167	DP3	99	IRQ7	67	SD13
5	D0	71	DRQ0	100	IRQ8#	68	SD14
6	D1	73	DRQ1	101	IRQ9	70	SD15
17	D10	76	DRQ2	4	LGNT0#	55	SD2
18	D11	79	DRQ3	174	LGNT1#	56	SD3
19	D12	80	DRQ5	158	LOCAL#	57	SD4
20	D13	82	DRQ6	41	LRDY#	59	SD5
21	D14	83	DRQ7	3	LREQ0#	60	SD6
22	D15	166	FERR#	173	LREQ1#	61	SD7
23	D16	146	FS1XCLK	116	MASTER#	62	SD8
25	D17	8	GND	111	MEMCS16#	63	SD9
26	D18	24	GND	113	MEMR#	49	SMEMR#
27	D19	52	GND	114	MEMW#	48	SMEMW#
7	D2	58	GND	1	nc	139	SPKR
28	D20	69	GND	2	nc	122	SYSCLK
29	D21	81	GND	43	nc	84	TC
30	D22	93	GND	44	nc	126	TURBO
31	D23	112	GND	45	nc	13	VCC
32	D24	145	GND	46	nc	35	VCC
33	D25	156	GND	87	nc	47	VCC
34	D26	159	HITM#	88	nc	74	VCC
36	D27	161	HLDA	89	nc	78	VCC
37	D28	162	HOLD	90	nc	103	VCC
38	D29	136	IDEBUFEN#	131	nc	125	VCC
9	D3	129	IDECS0#	132	nc	138	VCC
39	D30	130	IDECS1#	133	nc	147	VCC
40	D31	135	IDED7	134	nc	42	XDDIR
10	D4	165	IGNNE#	175	nc	120	ZWS#

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PicoPower Product Matrix

Type	Product	Part Number	Platform	Max DRAM	Integr. 206	Max. Freq. 5v/3.3V	Max. Freq. 3v	Int L2 Cache	VL IDE	Pins	Package
SCN	Evergreen	PT86C168	NB	64MB	N	33MHz	20MHz	N	N	208	PQFP
SCN	Evergreen HV	PT86C268	NB	64MB	N	33MHz	20MHz	N	N	208	PQFP
SCN	Pine	PT86C368	DT/NB	64MB	N	33MHz	20MHz	N	N	208	PQFP
SCN	Redwood 1	PT86C668	DT/NB	256MB	Y	50MHz	33MHz	Y	Y	160	PQFP
	Redwood 2	PT86C618	DT/NB	256MB	Y	50MHz	33MHz	Y	Y	160	PQFP
SCN	Redwood 1 (176)	PT86C768	DT/NB/SB	256MB	Y	50MHz	33MHz	Y	Y	176	TQFP
	Redwood 2 (176)	PT86C718	DT/NB/SB	256MB	Y	50MHz	33MHz	Y	Y	176	TQFP
SCN	Fir 1	PT86C868	NB/SB/E	64MB	Y	50MHz	33MHz	N	Y	144	TQFP
	Fir 2	PT86C818	NB/SB/E	64MB	Y	50MHz	33MHz	N	Y	144	TQFP
SCN	Cedar	PT86C378	NB/E	16MB	N	33MHz	25MHz	N	Y	208	PQFP
APT	PCMCIA Plus	PT82C786	ALL	n/a	n/a	50MHz	33MHz	n/a	n/a	100	TQFP

KEY: *Type*: SCN= System Controller; APT=Adaptor *Platform*: NB=Notebook; DT=Desktop; SB=Sub-notebook; E=Embedded

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REDWOOD/FIR Product Briefs

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40-509

Product Alert

Product	**REDWOOD / FIR**
Subject	**I/O Address Port 24H can not be read back reliably in some cases**
Date	**May 3, 1994**
Revision	**Rev 1.0**

The I/O port 24H is the index register for accessing Redwood/FIR internal registers, which can not be read back reliably in some cases. In general, all accessing of the Redwood/FIR internal registers is done during POST (Power On Self Test/Configuration Routine) and SMM routine. In these two cases, there is no cause for concern because there will be no requirement to read back and restore the content of I/O port 24H.

There is only one scenario within APM routine (shown below) which will cause the problem because of the I/O port 24H not being read back reliably.

< APM routine >
OUT 24H, XXH (INDEX)

SMI (Triggered)
<SMM Routine>
Store 24H's Index Before SMM Routine
:
: (Access Redwood/FIR internal
: registers through 24H - index, and
: 26H data port)
:
Restore 24H's Index Before Exit SMM Routine
RSM

OUT 26H, XXH (DATA)

If the 24H's index content can not be read back and restored correctly, then after the SMM routine, the immediate I/O write through 26H will be put into the wrong register. To work around this problem, BIOS vendors and programmers must implement soft shadow 24H port scheme to store the data content written to port 24H in an unused memory area, for example XBDA (Extended BIOS Data Area).

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With the shadow register scheme of I/O port 24H implemented, the corrected scenario is shown below:

Scenario With I/O Port 24H Soft Shadow Port Implementation

< APM routine >
Store INDEX of Port 24H to XBDA
OUT 24H, XXH (INDEX)

← SMI (Triggered)
<SMM Routine>
Save INDEX of Port 24H from XBDA
Before SMM Routine
:
: (Access Redwood/FIR internal
: registers through 24H - index, and
: 26H data port)
:
Restore INDEX of Port 24H back to Port 24H
Before Exit SMM Routine
← RSM

OUT 26H, XXH (DATA)

Future Stepping: This will be fixed on Rev A2 silicon.

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Redwood/FIR Chip Errata

Subj : Errata Summary of Redwood / FIR chipset

Date / Revision : 4/6/94 Rev 1.1

Below is the summary of all the errors found, causes and fixes, and stepping information on the bugs found.

1. Internal RTC failure

Redwood/FIR 1	Rev 0	Rev A0
	X	OK

Problem : Internal datapath error in RTC interface on Redwood/FIR 1

Workaround : Use external RTC (See Redwood Evaluation board schematic for details) for Rev 0 silicon. We are using a Dallas Semiconductor part DS12887/DS12887A.
Strap MA11 high through a 100K pull-up resistor. Three GPIO pins will then be converted to RTC interface signals :
GPIO0 = RWRTC
GPIO1 = DSRTC
GPIO2 = ASRTC

Stepping : This problem has already been fixed in Rev A0 silicon.

2. External RTC fails if Hidden ISA refresh is enabled

Redwood/FIR 1&2	Rev 0	Rev A0	Rev A1
	X	X	X

Problem : External RTC is controlled by Redwood/FIR 1 while hidden ISA refresh is controlled by Redwood/FIR 2 so that the refresh cycle may crash the RTC cycle initiated by Redwood/FIR 1.

Workaround : Set Reg 300H Bit 10 "ATREFDIS" to 1 to disable AT Refresh or use internal RTC with Rev A0, A1 silicon and onwards.

Stepping : Since Rev A1 will provide 128 bytes of CMOS RAM or ATREFDIS can be used with external RTC. There is no plan to fix this problem in Rev A1 and future silicons.

3. RDY# not generated for some CPU special cycles

Redwood/FIR 2	Rev 0	Rev A0
	X	OK

Problem : RDY# is not generated by Redwood/FIR 2 on some CPU special cycles. This causes system hang when INVD, Stop Grant and other special cycles are issued.

Workaround : Use an external PAL to generate the RDY# for special cycles with Rev 0 silicon.

Stepping : This problem has already been fixed in Rev A0 silicon.

4. RDY# not generated for DMA cycles if Reg 104H Bit 13 "ENRDY#" = 1

Redwood/FIR 2	Rev 0	Rev A0
	X	OK

Problem : If ENRDY# = 1, RDY# will not be generated at the end of the DMA transfer cycle, this will cause system hang. This problem has been fixed in Rev A0 silicon and DMA operation will be independent of ENRDY# bit setting.

Workaround : Set Reg 104H Bit 13 "ENRDY#" = 0 for Rev 0 silicon.

Stepping : This problem has already been fixed in Rev A0 silicon.

5. L2 Cache not working reliably at (2,1,1,1) if Reg 104H Bit 13 "ENRDY#" = 0

Redwood/FIR 1	Rev 0	Rev A0
	X	OK

Problem : If Reg 104H Bit 13 "ENRDY#" is set to 0 for DMA operation, the L2 Cache is not working reliably at (2,1,1,1). This problem has been fixed in Rev A0 silicon and L2 cache at (2,1,1,1) works reliably independent of ENRDY# bit setting.

Workaround : Set Reg 104H Bit 13 "ENRDY#" = 0 for Rev 0 silicon.

Stepping : This problem has already been fixed in Rev A0 silicon.

6. FRCSLW pin does not function

Redwood/FIR 1	Rev 0	Rev A0
	X	X

Problem : FRCSLW pin is not connected properly to the internal logic. This pin is an input to force the system to run at slower speed (by asserting STPCLK# signal) when the CPU overheat is detected by ext. thermocouple / comparator.

Workaround : No external fix in Rev 0 and A0 silicon.

Stepping : This will be fixed in Rev A1 silicon.

7. Problem with L2 WB Cache for memory accesses above 1MB

Redwood 1	Rev 0	Rev A0
	X	OK

Problem : Any memory accesses to XXXA0000-XXXBFFFF region above 1MB with L2 write-back cache mode will cause cache incoherency.

Workaround : Use L2 WT mode with Rev 0 silicon. This has been fixed for Rev A0/A1 silicon.

Stepping : This problem has already been fixed in Rev A0 silicon.

8. NMI will be generated even if there is no parity error

Redwood/FIR 2	Rev 0	Rev A0
	X	X

Problem : If parity is enabled, and if an AT cycle is immediately followed by a DRAM cycle, NMI will be generated even if there is no parity error in the DRAM cycle.

Workaround : Do not enable parity in Rev 0 and A0 silicon.

Stepping : This will be fixed in Rev A1 silicon.

9. QAFE timer test will fail and the program will be restarted and Norton SI / Norton Commander gives "Divide Overflow"

Redwood/FIR 2	Rev 0	Rev A0
	X	OK

Problem : The 8254 timer value is not updated when the timer is unlocked and locked again by the timer test program, giving a zero elapsed time and cause program failure.

Workaround : No external fix in Rev 0 silicon.

Stepping : This problem has already been fixed in Rev A0 silicon.

10. GPIO[4..7] can be written but cannot be read back

Redwood/FIR 2	Rev 0	Rev A0
	X	X

Problem : Internal logic bug. Fixed in Rev A1 silicon.

Workaround : No external fix in Rev 0 and A0 silicon.

Stepping : This will be fixed in Rev A1 silicon.

11. FLUSHWSMI bit does not work unless SMI pulse width is selected to 8 SCLKs

Redwood/FIR 1	Rev 0	Rev A0	Rev A1
	X	X	X

Problem : Logic error in Rev 0 and A0 silicon. For L1 WB CPU, registers will be saved to system memory during SMM. To avoid the write cycles hit the L1 WB cache, FLUSH# should be generated when SMI# is asserted instead of waiting for SMIACT# to be returned (as in L1 WT CPU). However, the system will hang when SMI# is asserted, if Reg 130H Bit 4 "FLUSHWSMI" = 1 and Reg 008H Bit 10 = 0.

Workaround : Set Reg 008H Bit 10 "SVNCLKPLS" to 1. This selects SMI# pulse width to 8 SCLKs which avoids the deadlock between FLUSH# and SMI#.

Stepping : There is no plan to fix this problem in Rev A1 or future silicon.
Just set Reg 008H Bit 10 = 1 to fix the problem for all silicon revisions.

12. Port 92 Fast RC and Fast A20GATE functions only if 8042 RC# and A20GATE not used

Redwood/FIR 1	Rev 0	Rev A0
	X	X

Problem : If the KBRST# and/or A20GATE input of Redwood/FIR 1 are used (from 8042), the Port 92 Fast RC# and Fast A20GATE function will be disabled correspondingly, which is incorrect.

Workaround : Do not use 8042's RC# and A20GATE input. Select the pin function other than KBRST# and A20GATE input and the Fast RC and A20GATE function will be automatically enabled. (That is Reg 111H Bit 8 should be set to 1)

Stepping : This will be fixed in Rev A1 silicon.

13. Reg 110H Bit 5 is not overriden by Reg 100H Bit 0 = 1

FIR 1	Rev 0	Rev A0
	X	X

Problem : PC[4..9] will not be automatically selected by strapping MA0A = 1. This is because Reg 110H Bit 5 "TAGDEN", which should be, is not being overriden by Reg 100H Bit 0 = 1 which implies FIR mode.

Workaround : Program Reg 110H Bit 5 = 1 for FIR mode to enable PC[4..9]

Stepping : This will be fixed in Rev A1 silicon.

14. MA[7..9] if strapped randomly, will cause system hang

Redwood/FIR 1	Rev 0	Rev A0
	X	X

Problem : MA[7..9], or Misc. Config [0..2], cannot be strapped randomly for customized applications as intended, but has to stay at [000] for Rev 0 and A0 silicon.

Workaround : Do not use MA[7..9] for developement purposes.

Stepping : This will be fixed in Rev A1 silicon.

15. Reg 01DH Bit [8:11] malfunction

Redwood/FIR 1	Rev 0	Rev A0
	X	X

Problem : Reg 01DH Bit [8:11] are supposed to provide individual control for programmable timers 0-3. However, in Rev 0 and A0 silicon, whenever Reg 006H Bit 12, IMSKPROGTO is unmasked, all timers will generate PMI when they time out, disregarding the programmed value in Reg 01DH Bit [8:11].

Workaround : Disable those timers which are not used to trigger SMI.

Stepping : This will be fixed in Rev A1 silicon.

System Level Precaution

1. **If L2 is in WB mode and 0 WS DRAM write is selected, the system will hang**

   This is because a L2 Write Hit should not start a DRAM cycle. However, if 0WS DRAM write is selected, the DRAM state machine have to start at the beginning of 1st T2, together with L2 for the write hit cycle, which causes system hang. For L2 WT mode, it is working OK.

   Summarizing,

   L2 WT at (2,1,1,1) : DRAM should be no faster than 1 WS READ, 0 WS WRITE.
   L2 WB at (2,1,1,1) : DRAM should be no faster than 1 WS READ, 1 WS WRITE.

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Redwood/FIR Application Note

Abstract : **Correct POWER PLANE usage of Redwood/FIR-based design and some related issues**

Date / Revision : **03/31/94 Rev 1.0**

There are some recent design changes in the Redwood / FIR internal power plane structure which may affect system designs. Also, there have been many questions about how to connect the power planes of Redwood/FIR 1 & 2 to the power supply and what planes should be On or Off during Standby, Suspend, Full-On etc. This document is created to addressed this and other related issues pertaining to Power Sequencing, PWRGOOD etc.

[To simplify the discussion, unless otherwise stated, FIR will be used to represent both Redwood/FIR since they shared the same voltage plane architecture and PG will be used as abbreviation for PWRGOOD.]

Power Planes in Redwood/FIR

FIR has a very flexible power plane structure in order to meet the requirements of various system architectures, including Desktop, Notebook, systems supporting either 0V-Suspend/Resume, 5V-Suspend/Resume etc. FIR 1 has a core voltage plane named VDD_CL and five I/O planes named VDD_IOx (where x = 1 to 5). FIR 2 has a core voltage plane also named VDD_CL and three I/O planes named VDD_IOy (where y = 1, 3 and 4). **The following discussion will be non-specific to 5V, 3V or hybrid system, however, an important criteria for FIR-based system design is that, VDD_CL's voltage must be equal or higher than any other VDD_IO planes in the same chip.** Once this criteria is meet, you can design a FIR-based hybrid system without other voltage plane combination limitations.

We will use the following naming convention throughout the document :

	Redwood	FIR
VDD_CL	Core Logic power group	Core Logic power group
VDD_IO1	CPU interface	CPU interface
VDD_IO2	DRAM interface	DRAM interface
VDD_IO3	ISA, PC[0:3], Misc interface	ISA, PC[0:3], Misc interface
VDD_IO4	BBUS interface	BBUS interface
VDD_IO5	L2 Cache interface	PC[4:9], PMC interface

Please note that FIR 1 VDD_CL is shared between RTC and other high speed logic, therefore, VDD_CL should be powered by main battery during normal operation and by RTC backup battery during Standby state.

System Terminology

STR = Suspend-To-RAM = 5V-Suspend
STD = Suspend-To-Disk = 0V-Suspend, this is effectively the same as system Off or Standby state
SSP = Static Suspend = All clock stopped (except 32KHz) with most devices powered-on

Redwood & FIR

VDD_MAIN Either 3V or 5V, it will be Off during STR.
VDD_SUSP Either 3V or 5V, it will be Off during Standby mode or STD.
VDD_ALWAYS Either 3V or 5V, it will be On even if the system is powered-off, either through a high-efficiency DC/DC converter from the main / secondary system battery, or even RTC backup battery.

For typical FIR-based designs, the following will apply :

	Redwood 1 / FIR 1	Redwood 2 / FIR 2
VDD_CL	VDD_ALWAYS	VDD_MAIN
VDD_IO1	VDD_MAIN	VDD_MAIN
VDD_IO2	VDD_SUSP	N.A.
VDD_IO3	*VDD_ALWAYS / VDD_SUSP	VDD_MAIN
VDD_IO4	VDD_MAIN	VDD_MAIN
VDD_IO5	VDD_SUSP / VDD_MAIN	N.A.

Microcontroller (51SL, H8, 38802)	VDD_ALWAYS	: if uC is On all the time (most popular approach)
	VDD_SUSP	: if uC is On during Suspend, Off during Standby
	VDD_MAIN	: if uC is Off during Suspend and Standby

*Remarks : *VDD_IO3 of Redwood / FIR 1 needs to be VDD_ALWAYS for Rev 0 and A0 silicon. This has been changed in Rev A1 silicon and VDD_IO3 can be either On or Off during Standby*

As can be seen, FIR 2 is pretty easy to deal with since FIR 2 are mainly a VL and ISA interface chip, and those devices are mostly powered-off or power-down during Suspend, thus FIR 2 should also be powered-off during Suspend and all its power planes should be connected to VDD_MAIN. For this reason, FIR 2 does not require any leakage control circuit on-chip.

Most flexibility lies in the FIR 1. As the RTC is inside the FIR 1 core and its content is kept by VDD_CL, therefore, FIR 1 VDD_CL needs to be always On, minimum recommended to be 3V, either by RTC_BATT, MAIN_BATT (through DC/DC) or secondary system battery. It is pretty obvious that FIR 1's VDD_IO1 and VDD_IO4 should be powered-off during STR since CPU and FIR 2 are Off. VDD_IO2 however, must be kept On during STR since it is required to keep system DRAM refreshed. VDD_IO3, which powers the PC[0:3], should be kept On during STR since it needs to drive PC[0:3] to keep other system devices On/Off. VDD_IO5 is a special case, in Redwood, it is the L2 Cache interface power plane. In FIR, however, it is the PMC interface power plane. If the L2 Cache in Redwood design is Off or the PC[4:9] in FIR design is not used during STR, VDD_IO5 can be

connected to VDD_MAIN. However, if L2 Cache is kept On during STR, or PC[4:9] are being used for power control functions during STR, VDD_IO5 should be connected to VDD_SUSP.

Nowadays, many systems utilize a microcontroller (uC) to perform centralized control for various important, but not speed-critical system events to achieve a consistent and programmable interface to the system controllers, eg., FIR. Those events are such as Power Switch, Lid Switch, Susp/Resume Switch (make and break), Battery Charging & monitoring, Keyboard scanning, ADC/DAC for temperature, voltage sensing and brightness/contrast control etc etc. Such uC doesn't need to be fast, however, flexible and low power are the main concerns. In some designs, the uC even provides the necessary timing relationship between 5V, 3V power and PWRGOOD assertion and deassertion.

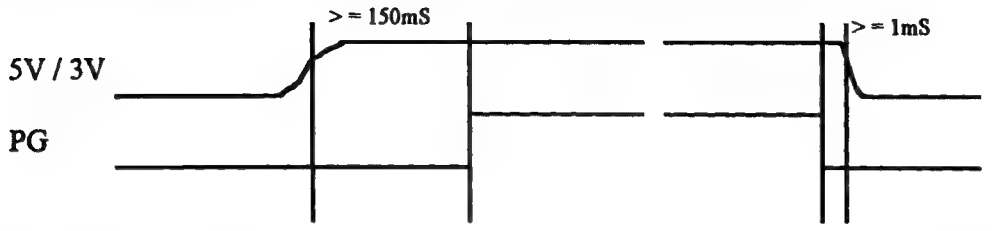
IMPORTANT Changes related to Wakeup Control signals that may affect system designs

The original design target of FIR is to allow wakeup inputs to function properly without powering on the corresponding VDD_IOx plane. However, this needs to be changed to, whenever a particular wakeup pin is used, either SWTCH, RING, WAKE0 or WAKE1, its corresponding VDD_IOx plane, must also be powered On in order to resume from STR. ***This is different from earlier recommendation, please do the proper adjustment to the design.***

	Voltage Plane
SWTCH (Redwood)	VDD_IO3
SWTCH (FIR)	VDD_IO5
RING (Redwood)	VDD_IO3
RING (FIR)	VDD_IO5
WAKE0	VDD_IO5
WAKE1	VDD_IO1

Also, there is a lot of confusion whether the wakeup signals can wakeup FIR from Standby state. The answer is, PWRGOOD is the only recommended wakeup source from Standby state to Fully-On mode. All other wakeup sources are mainly for Suspend / Resume operation to/from STR. If wakeup from STD is required as a system specification, a microcontroller is recommended to monitor all wakeup events so that it can trigger a wakeup source of FIR to resume from STR or turn on the DC/DC converter and generate PG at proper time to resume from STD.

Recommended Timing relationship (for both Desktop and Notebook applications)



The recommended timing requirement for PG is pretty simple and is almost the same as regular PC/AT power supply. It is recommended that PG is asserted "H" at least 150mS (PwrOnTPGH or Power On To PG "H") after both 5V and 3V are stabilized, to allow enough time for CPU and system reset. When the system is powering off, PG should be deasserted at least 1mS (PGLTPwrOff or PG "L" To Power Off) before either 5V or 3V drop to their -10% margin so that FIR can enter Standby state (RTC data retention state or the lowest power state) before the system power goes away.

In FIR design, PG is a primary indicator of system power On or Off and by default, whenever PG is "L", FIR will enter Standby state in order to prevent draining excessive power from the RTC Backup battery (if it stays in Fully-On mode). The behaviour can be changed by setting Reg 013H Bit [2:3] though, please refer to Redwood/FIR data book for details.

Difference between FIR and PINE's PG behaviour

In PINE, the RTC is physically located inside the 82C206 so that PG is used to enable the leakage control of 82C206. PINE will automatically enable leakage control whenever the BIOS programs its Reg 001H Bit [13:15] to Suspend or Standby mode. Actually, in PINE, we recommend to use one of the PCx to pull PG to "L" as fast as possible in order to turn on the '206 leakage control in the shortest possible time. Therefore, PG is "L" during STR in a PINE design.

In FIR, however, PG is used very differently. To avoid driving FIR into Standby standby state when PG goes "L", PG has to stay "H" during STR. In Rev 0 and A0 silicon, PG is always debounced and has 12-16mS debounce time on both rising edge or falling edge of PG. The debounce is used to avoid a sudden power surge (thus glitch on PG) which will put the system into Standby mode, however, there is a potential issue with the falling edge debounce, though. Therefore, in Rev A1 silicon, we have added a new programmable bit, named, **NPWRGDDBDIS** (falling edge PG debounce Disable) in Reg 110H Bit 0. NPWRGDDBDIS is defaulted to "0" (on RCRST# rising edge) which provides 12-16mS debounce time on PG falling edge. If the bit is set to "1", PG debounce will be "Disabled". It is default debounced mainly for backward compatibility, however, it is recommended that BIOS should always set Reg 110H Bit 0 to "1" and the system design has to guarantee that PG does not glitch, otherwise, FIR will enter Standby mode.

Followings are some examples for designers' reference on various system scenarios on systems based on Redwood/FIR, for both Desktop and Notebook. Designers can change according to their needs and their specific system architecture. A common misconception is that, since FIR1 and FIR2's VDD_CL and VDD_IOx are exactly the same name, they should be tied together, this is incorrect and the tables below will clarify that.

SCENARIO #1 : Desktop System using regular Power Supply

System assumption : The system supports only Static Suspend, use low cost 8042.
PG is generated by power supply.

	Redwood 1 / FIR 1	Redwood 2 / FIR 2
VDD_CL	VDD_ALWAYS	VDD_MAIN
VDD_IO1	VDD_MAIN	VDD_MAIN
VDD_IO2	VDD_MAIN	N.A.
VDD_IO3	*VDD_ALWAYS / VDD_MAIN	VDD_MAIN
VDD_IO4	VDD_MAIN	VDD_MAIN
VDD_IO5	VDD_MAIN	N.A.

8042 Keyboard controller	VDD_MAIN

Clock Sythnsizer (except 32KHz) HDD, FDD	Off during Static Suspend
VGA	enter VESA DPMS (Display Power Management) Suspend mode

*Remarks : *VDD_IO3 of Redwood / FIR 1 needs to be VDD_ALWAYS for Rev 0 and A0 silicon.*
This has been changed in Rev A1 silicon and VDD_IO3 can be Off for desktop design during Standby

SCENARIO #2 : Notebook System using REDWOOD with L2 Cache

System assumption : The system supports both STR and STD, WAKE0/1 not used.
PC[0:3] are used. L2 is Off during STR.
uC is used as a central controller monitoring all wakeup events during STR.
uC is used as power On/Off controller.
System can wakeup from STD by a momentary switch.

	Redwood 1 / FIR 1	Redwood 2 / FIR 2
VDD_CL	VDD_ALWAYS	VDD_MAIN
VDD_IO1	VDD_MAIN	VDD_MAIN
VDD_IO2	VDD_SUSP	N.A.
VDD_IO3	*VDD_ALWAYS / VDD_SUSP	VDD_MAIN
VDD_IO4	VDD_MAIN	VDD_MAIN
VDD_IO5	VDD_MAIN	N.A.

Microcontroller	VDD_ALWAYS

*Remarks : *VDD_IO3 of Redwood / FIR 1 needs to be VDD_ALWAYS for Rev 0 and A0 silicon.*
In Rev A1 silicon, VDD_IO3 should be On during Suspend, Off during Standby.

SCENARIO #3 : Notebook System using FIR (supports STR but not STD)

System assumption : The system supports STR but not STD, WAKE0 and WAKE1 used.
PC[0:3] are used and PC[4:9] are optionally used.
uC is used as a central controller monitoring all wakeup events during STR.
uC is used as power On/Off controller.

	Redwood 1 / FIR 1	Redwood 2 / FIR 2
VDD_CL	VDD_ALWAYS	VDD_MAIN
VDD_IO1	VDD_SUSP since WAKE1 used	VDD_MAIN
VDD_IO2	VDD_SUSP	N.A.
VDD_IO3	*VDD_ALWAYS / VDD_SUSP	VDD_MAIN
VDD_IO4	VDD_MAIN	VDD_MAIN
VDD_IO5	VDD_SUSP since WAKE0 used	N.A.

Microcontroller	VDD_ALWAYS

*Remarks : *VDD_IO3 of Redwood / FIR 1 needs to be VDD_ALWAYS for Rev 0 and A0 silicon.*
In Rev A1 silicon, VDD_IO3 should be On during Suspend, Off during Standby.

SCENARIO #4 : Notebook System using FIR (supports both STR and STD)

System assumption : The system supports both STR and STD, WAKE0/1 not used.
PC[0:3] are used and PC[4:9] are optionally used.
uC is used as a central controller monitoring all wakeup events during STR.
uC is used as power On/Off controller.
System can wakeup from STD by modem ring.

	Redwood 1 / FIR 1	Redwood 2 / FIR 2
VDD_CL	VDD_ALWAYS	VDD_MAIN
VDD_IO1	VDD_MAIN	VDD_MAIN
VDD_IO2	VDD_SUSP	N.A.
VDD_IO3	*VDD_ALWAYS / VDD_SUSP	VDD_MAIN
VDD_IO4	VDD_MAIN	VDD_MAIN
VDD_IO5	VDD_SUSP if PC[4:9] used VDD_MAIN if PC[4:9] not used	N.A.

Microcontroller	VDD_ALWAYS

*Remarks : *VDD_IO3 of Redwood / FIR 1 needs to be VDD_ALWAYS for Rev 0 and A0 silicon.*
In Rev A1 silicon, VDD_IO3 should be On during Suspend, Off during Standby design during Standby.

In scenario #4, since the uC supports wakeup from STD by modem ring, that means it has to monitor RI# output from RS232 driver and when the necessary conditions are met (eg. # of rings), it will then power up the system and generate PG to wakeup FIR from Standby state.

Following four diagrams are the typical Power Up / Down and Suspend / Resume sequences for either Redwood or FIR based design, for designers' reference.

Note : there is no absolute requirement between the 5V and 3V power up/down timing, but it will be beneficiary if during power On, 5V plane can be turned on and stabilize a short period of time (eg 1mS) before 3V plane. And for similar reason, during power Off, 3V plane can be turned off and a short period of time (eg 1mS) before 5V plane.

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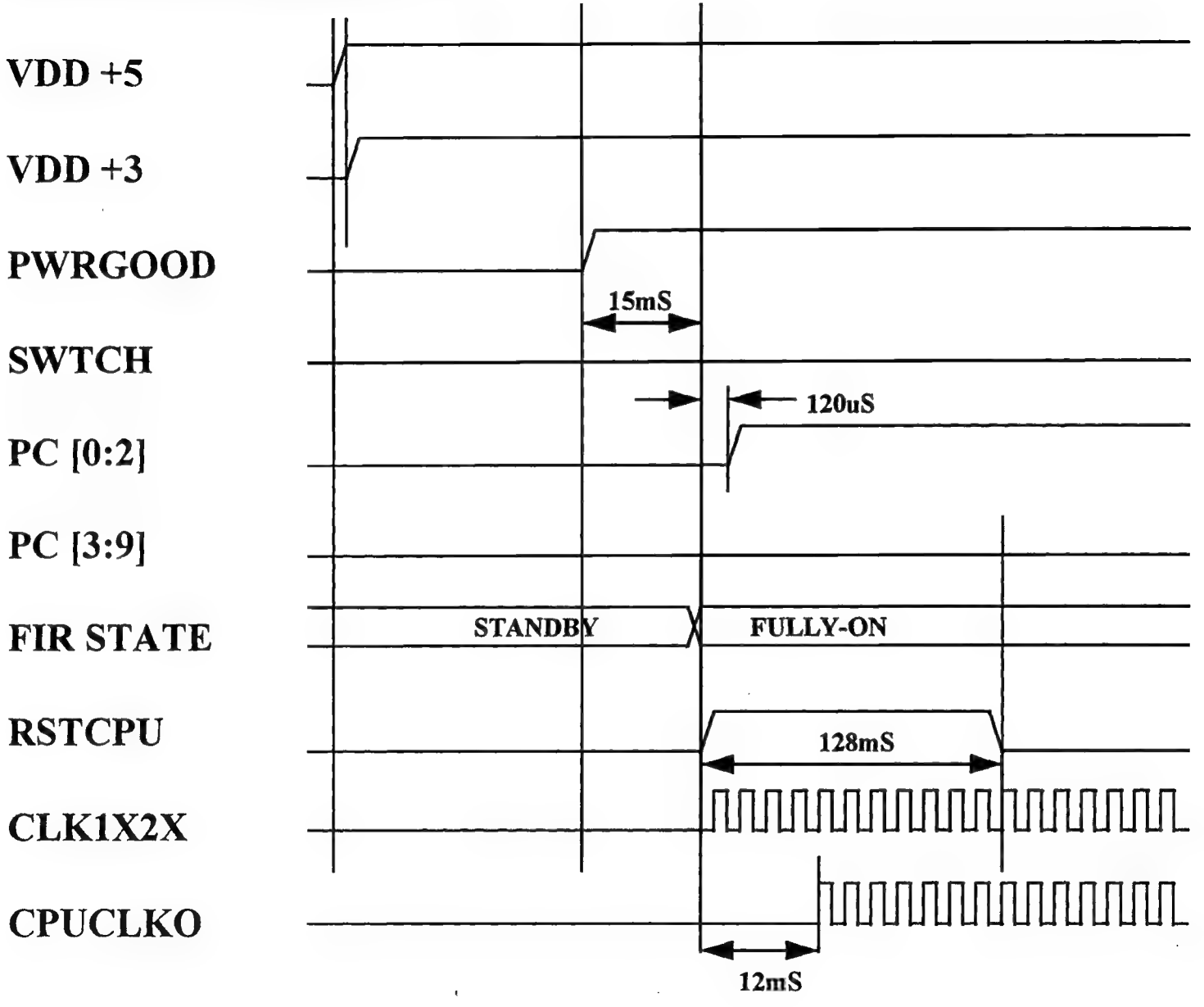
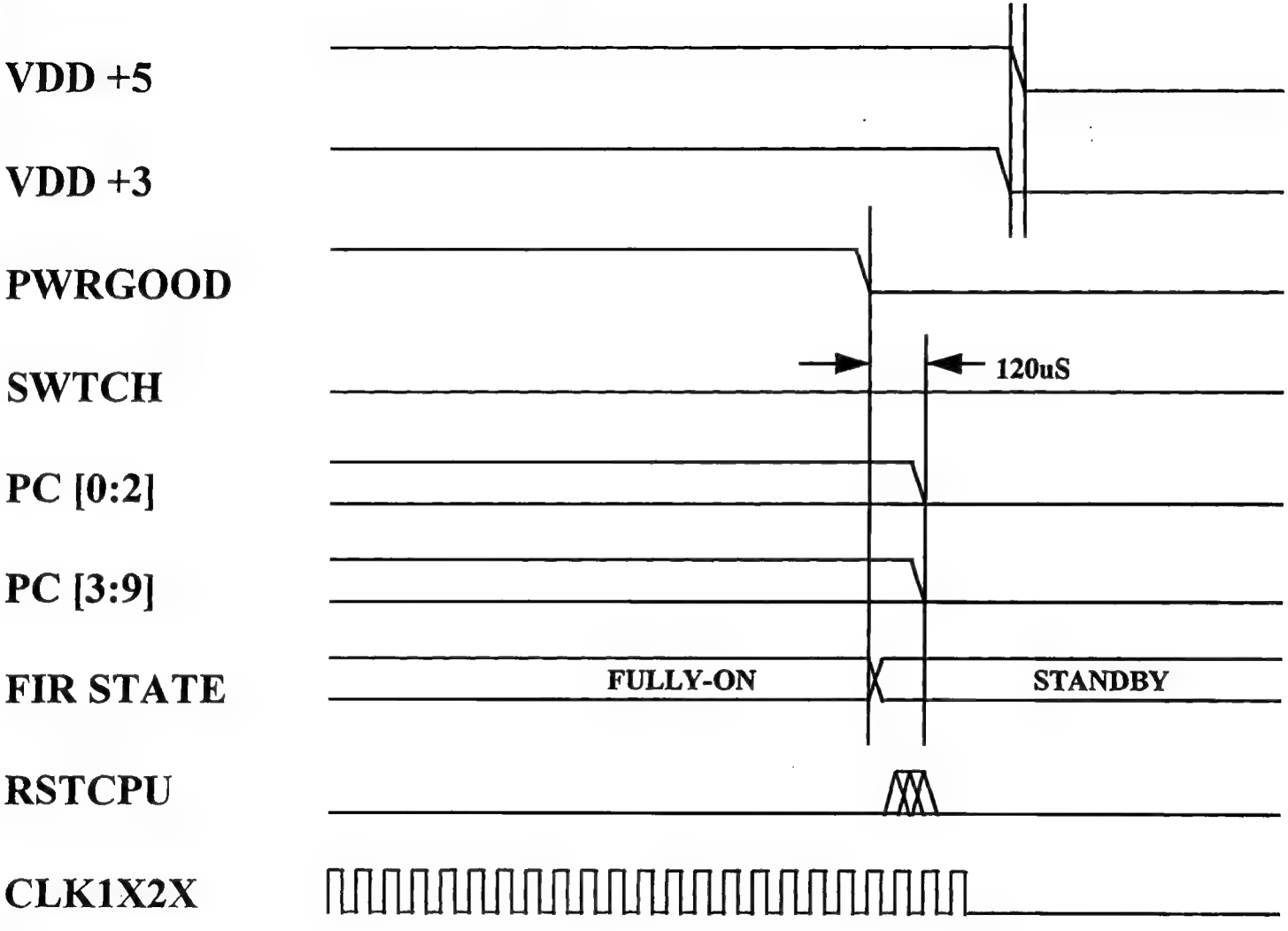
POWER UP SEQUENCE

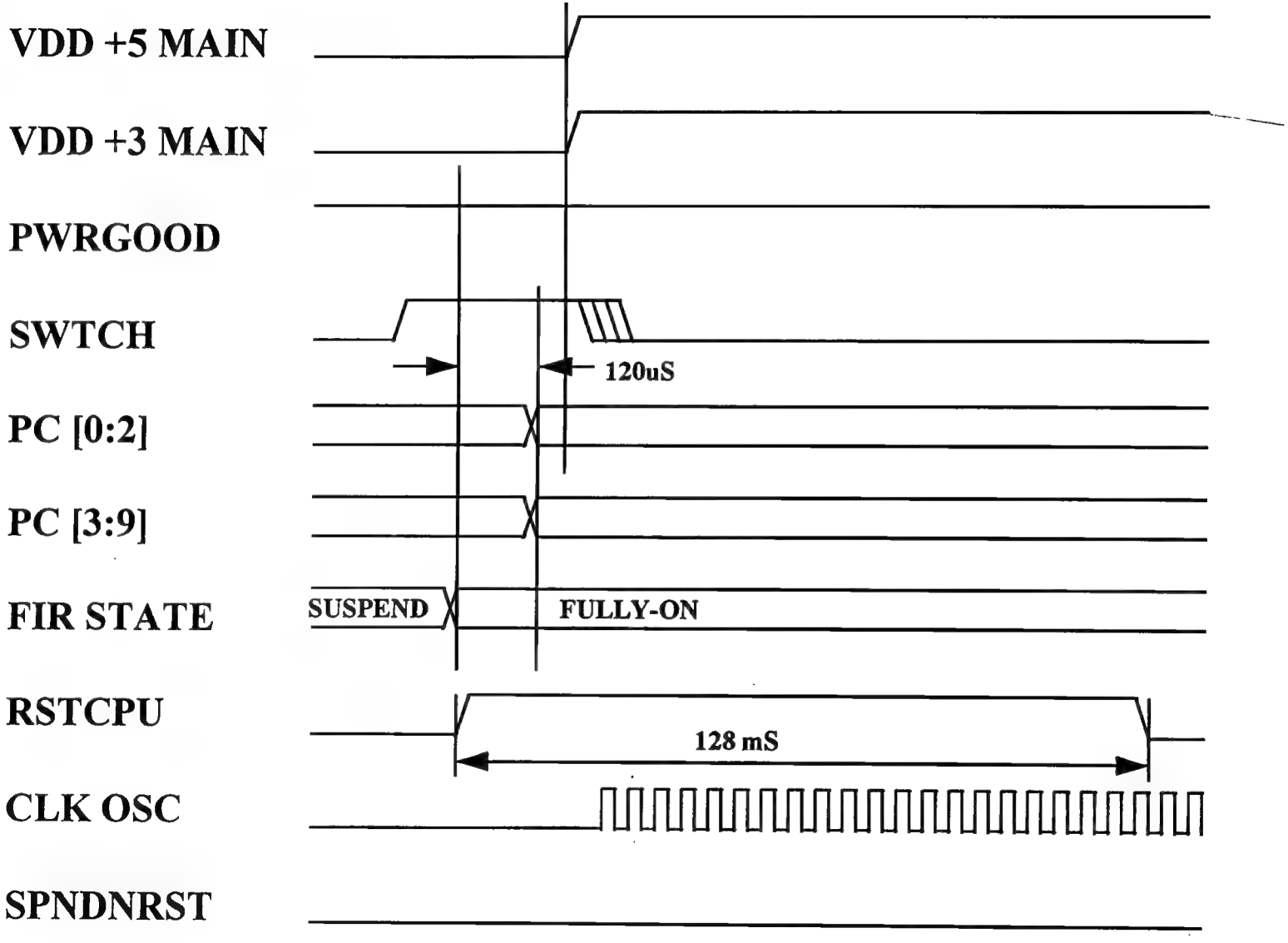


POWER DOWN SEQUENCE

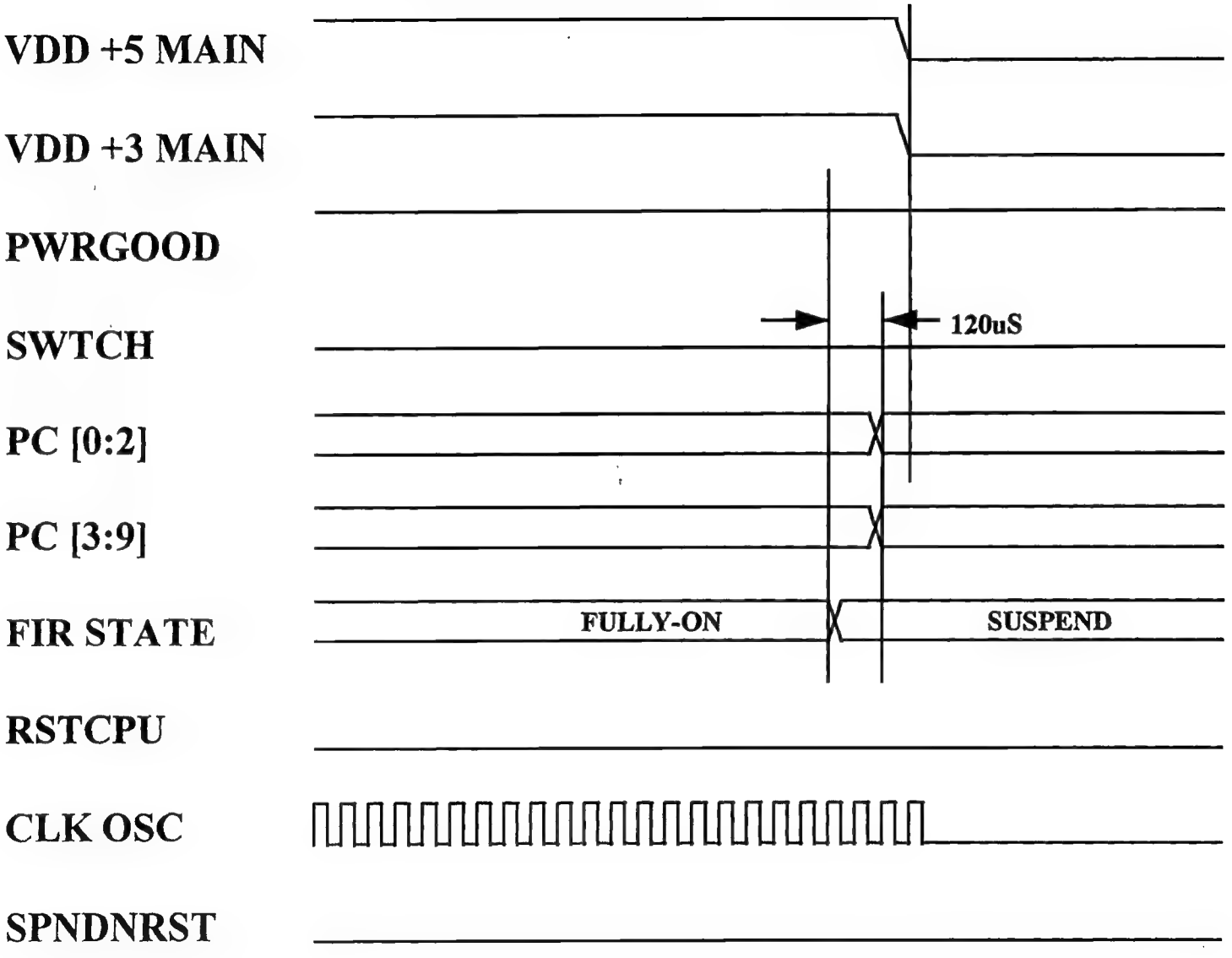


CONDITION : REG 110H Bit 0, NPWRGDDBDIS = 1

RESUME SEQUENCE



SUSPEND SEQUENCE



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Redwood/FIR Application Note

Abstract : **'Static Suspend' mode on Redwood / FIR**

Date / Revision : **02/18/94** **Rev 1.0**

'Static Suspend' Definition:

REDWOOD / FIR supports a new mode known as 'Static Suspend'. For CMOS devices, the power consumption is directly proportional to the operation frequency driving the device. 'Static Suspend' is making the best use of this characteristic so that, if we totally stop the clock to all the devices in the system, the system should consume minimum amount of power (if the static Idd is not excessive). Since 'Static Suspend' does not require powering-up and down the devices in the system (except LCD, FDD, and HDD, etc.), it greatly simplifies the power switching design and can avoid the painful process of resuming a non-standard ISA add-on card to its state before suspend, which makes 'Static Suspend' not only suitable for Notebook applications, but also an attractive alternative in Green PC design.

Another advantage of 'Static Suspend' is, as all devices are kept powered-on, it greatly simplifies the leakage control consideration inside the system. REDWOOD / FIR provides a bit, LCDIS or Leakage Control Disable (Reg 015H bit 15) to disable leakage control circuitry upon entering suspend mode.

Below are the instructions on how to use 'Static Suspend' Mode.

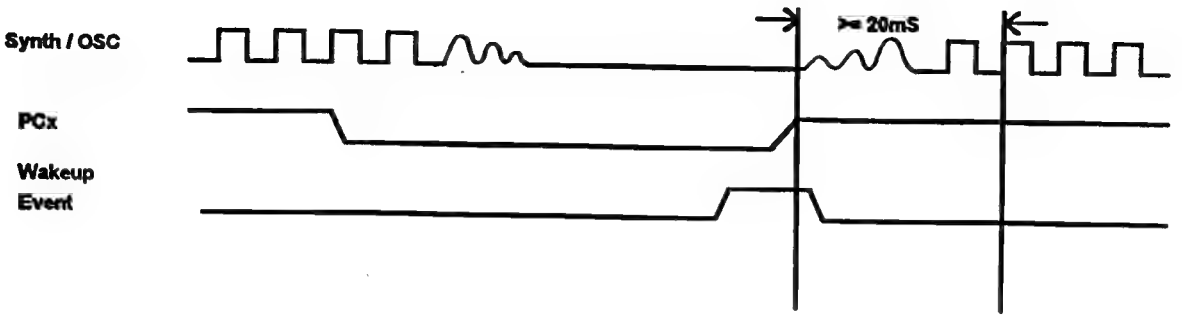
Before entering 'Static Suspend'.

- Select 'More Stop' option for CPU STPCLK control during Suspend.
- Disable system leakage control.
- Set the 'PCx' properly to turn off devices like HDD, FDD, LCD and OSC.
- Miscellaneous steps like setting "Mode Change Immediate", "Disable RSTDRV and RSTDRV upon resume" since all devices are powered and should not be reset.
- Set 'Start Delay' to 30mS - 60mS.
- Put the video and other devices to their low power state if possible
- Enter Suspend Mode (hardware should keep PWRGOOD "H" during 'Static Suspend').

Resuming from 'Static Suspend'.

- The chip will wait for the 'Start Delay' which is 30-60mS to allow the clock to stabilize.
- The stabilize clock then 'gated' to the internal clock machine of REDWOOD / FIR.
- The system will be resumed while the CPU is still in SMM mode.
- If the video and other devices are put to their lowest power state before Static Suspend, during resume, software (either the batch file or BIOS) should bring those devices back to the original state before system operation can continues.
- The BIOS will perform any house cleaning necessary.
- Execute 'RSM' instruction and back to business.

The typical timing for Entering / Exiting 'Static Suspend'.



Following is the sample program that shows how 'Static Suspend' mode works. This program can be run as a batch file, and it is for testing purpose only. The actual code for 'Static Suspend' should be in the BIOS.

Entering Static Suspend Mode

CFW	00E	F800	-	Mask GP Timer from waking up system (Reg 00EH bit <11> = 1), just in case
CFW	301	407F	-	Enable BSER bit (Reg 301H bit <14> = 1)
CFW	118	010A	-	Set Reg 118H bit <1> = 1 to stop CPUCLK during STPCLK state Set Reg 118H bit <8> = 1 to enable 'Mode Change Immediate'
CFW	008	008F	-	Set Reg 008H bit <0> = 1 to enable Stop Clock Global Set Reg 008H bit <1> = 1 to enable More Stop Set Reg 008H bit <3:2> = 3H for 1mS STPCLK Release Delay Set Reg 008H bit <7> = 1 to wait for Stop Grant Cycle
CFW	015	80FF	-	Set Reg 015H bit <15> = 1 to disable the Leakage Control
CFW	00A	088F	-	Set Reg 00AH bit <11> = 1 to set the 'Start Delay' to 30-60mS
CFW	**013**	**0180**	-	**Set Reg 013H bit <7> = 1 to disable asserting RSTCPU upon resume** **Set Reg 013H bit <8> = 1 to disable asserting RSTDRV upon resume**
CFW	001	000A	-	Enter Suspend mode

Note: CFW & CFR are PicoPower Ultility Program which write and read REDWOOD / FIR registers.
Note: Reg 013H Bit 7 and 8 are confidential"reserved" bits and are useful only for Static Suspend and Resume
Note: Some of the bit patterns above are used such that they work with the Redwood/FIR evaluation board. If designers are testing Static Suspend in their own platform, the bit values should be changed correspondingly.

Resuming from Static Suspend Mode

Press the Switch to return to ON mode.

Below are the definition of each bit that is used in 'Static Suspend' example as shown above :

Register	Bit	Name	Functions
301H	14	BSER	**BSER Enable:** When high, BSER function to REDWOOD2/FIR2 will be enabled. When low, BSER will stay high always and the function will be disable.
118H	1	VLCLKSTPEN	**VL Clock Stop Enable:** If high, VLCLK (CPUCLKO1) will be stopped during Stop Clock State. If low, it is always running.
118H	8	MDCHGIMD	**Mode Change Immediate:** When high, PMC mode changes will occur immediately upon request; when low, mode changes will only occur at the end of a CPU Bus cycle or when the CPU Bus is idle.
008H	0	STPGLBEN	**Stop Clock Global Enable:** When high, an appropriate stop clock protocol will automatically be applied upon detection of any request to change the frequency of or to stop the CPU clock.
008H	1	MORESTOP	**More Stop:** When high, and when STPGLBEN (bit 0 above) is also high, the CPU clock will be stopped upon detection of a Stop Grant cycle. When low, the CPU clock frequency will remain constant in the Stop Grant state. SLWCLKDIV set to STOPPED.
008H	<3:2>	STPRELDLY <1:0>	**STPCLK Release Delay** (PLL Stabilization Delay): This parameter defines the delay between restarting the CPU clock and de-asserting STPCLK. Please see the REDWOOD register spec. for further detailed.
008H	7	WAIT4GRNT	**Wait for Stop Grant:** When high, any assertion of STPCLK will be held at least until a Stop Grant Cycle is received. When low, STPCLK may be deasserted prior to a Stop Grant Cycle.
00AH	11	STRTDLY	**Start Delays:** When high, the CLK1X2X input will be internally latched for 30mS to 60mS following each resume. When low, the internal clock will immediately follow CLK1X2X upon any resume.
00EH	11	WMSKTMR	**Wake Mask GP Timer:** When high, a compare on the GP Timer will not trigger a wake-up from Suspend or Standby modes. When low it will.
013H	*7*	*Reserved SPRSTCPUDIS*	***Disable RSTCPU upon Resume: When low, RSTCPU will be asserted upon Resume. When high, RSTCPU will not be asserted***
013H	*8*	*Reserved SPRSTDRVDIS*	***Disable RSTDRV upon Resume: When low, RSTDRV (also RSTDRV#) will be asserted upon resume. When high, RSTDRV will not be asserted.***
015H	15	LCDIS	**Leakage Control Disable:** When high, no leakage control circuitry will be engaged upon entering Suspend. When low, leakage control will automatically be engaged on entering Suspend.

----- End of Document -----

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Redwood/FIR Application Note

Abstract : **Redwood/FIR Leakage Control**
Date / Revision : **2/18/94** **Rev 1.0**

PINE	REDWOOD	FIR
—	☺ A0 onward	☺ A0 onward

☺	= Applicable
☹	= Not Applicable
—	= Function Not Available

Redwood/FIR, due to their very special buffer design, uses an advanced yet simple leakage control mechanism which will benefit all next generation notebook designs based on them. Almost all existing notebook chipsets have some kinds of leakage control to drive some signals either high or low during Suspend mode to avoid :

1. an ON device driving a signal "H" to an OFF device whose protection diode may clamp the signal to GND
2. leakage current due to floating input to an ON device, due to the partially On CMOS buffer gate

With the special input buffer design, Redwood/FIR can isolate the input completely during Suspend so that, there will be no leakage current even if the input is floating. This implies if Redwood/FIR I/O pin's output buffer is tristated during Suspend, its input buffer will not leak as it is completely isolated from the outside world.

The result ? We can *tristate* all Output and I/O pins on Redwood 1 during Suspend while the Redwood 2 can *be (and should be)* powered off completely during Suspend. Attached is a table detailing all the pin status during Full-On, Suspend mode, which will be very helpful for system designers.

The following tables show the signal's Grouping, Power Plane on RW/FIR, buffer type and Idle state, Suspend Pin state and requirements for external pull-up or pull-low resistors. By Suspend state, we refers to 3V-Suspend or 5V-Suspend state but not 0V-Suspend, since 0V-Suspend is functionally equivalent to System Off with the system state saved.

An *important remark* about the Suspend Pin state is, "OUTPUT" pins are "Hi-Z" if the corresponding leakage control groups are enabled. Leakage control for groups like DRAM, PC, GPIOs etc can be individual disabled so that they can properly refresh the DRAM, and control external DC/DC converter during Suspend state. Refers to Rev 2.1P Specification Reg 015H for details.

LEGEND USED :

Hi-Z	=	**High Impedance or 3-State**
X	=	**Indeterminate in Output mode (may be software dependent like A20M#)** **Don't Care in Input mode**
Input	=	**The pin(s) is at Input mode, usually they are Address, Data and Cycle decode signals from CPU.**
PD	=	**Pull-Down**
PU	=	**Pull-Up**

REMARKS :

(a) RCRST#, PWRGOOD, 32KIN are always active.
(b) Wake-up source: SWTCH, RING, WAKE0, WAKE1 and IRQ8# (input mode) are always active.
(c) MA: used as reset sampling. Normally output mode. Switched to input mode only during reset. Must be tristated during RCRST# or PWRGOOD "L" for proper sampling.
(d) All EXTACT's, GPIO's should be externally pulled or tied low if not used.
(e) PC0-PC3 should drive only capacitive loads to avoid draining the backup battery.

REDWOOD 1 LEAKAGE CONTROL PIN STATUS

Group/ Plane	Pin Name	Operating State (Full-On, Doze, Sleep)		Suspend State	Remarks and Ext PU/PD Requirements
CPU Interface		TYPE	Idle State	Pin State	
CPU/1	A<27:2>	I/O	Input	Hi-Z	PD on A<30:28> required for RW PD on A<30:26> required for FIR
CPU/1	A31	I/O	Input	Hi-Z	--
CPU/1	BE<3:0>#	I/O	Input	Hi-Z	optional PU
CPU/1	ADS#	I/O	Input	Hi-Z	PU
CPU/1	RDY#	I/O	Hi-Z	Hi-Z	PU (tristate, bidirectional)
CPU/1	BRDY# (PEREQO)	I/O O	Hi-Z L	Hi-Z Hi-Z	PU (tristate, bidirectional) --
CPU/1	BLAST# (BUSYO#)	I O	H H	Hi-Z Hi-Z	optional PU --
CPU/1	M/IO#	I/O	Input	Hi-Z	--
CPU/1	D/C#	I/O	Input	Hi-Z	--
CPU/1	W/R#	I/O	Input	Hi-Z	--
CPU/1	EADS# (ERRORO#)	I/O O	H H	Hi-Z Hi-Z	PU --
CPU/1	KEN#	O	L	Hi-Z	--
CPU/1	HLDA	I	L	-	--
CPU/1	A20M#	O	X	Hi-Z	--
CPU/1	SMIACT# (SMIADS#)	I I	H H	- -	optional PU PU
CPU/1	FLUSH# (IRQ13)	O O	H L	Hi-Z Hi-Z	-- --
CPU/1 AT/1	SMI# (PMI/IRQ)	I/O O	H L	Hi-Z Hi-Z	PU (10K nom., 330 ohm for specific CPU) --
CPU/1 PM/1	NMI (EXTACT0)	I I	L L	- -	PD if not used to monitor NMI from RW/FIR2 PD if not used
CPU/1	STPCLK#	O	H	Hi-Z	--
CPU/1	SRESET	O	L	Hi-Z	--
CPU/1	HITM# (ERRORI#)	I I	H H	- -	PU PU if 387 not used
CPU/1	LOCK# (CA13) (TAGCS#) (BUSYI#)	I O O I	H X H H	- Hi-Z Hi-Z -	optional PU -- -- PU if 387 not used
CPU/1	CACHE# (PEREQI)	I I	H L	- -	PU --
CPU/1	WB/WT# (SMIRDY#)	O O	H H	Hi-Z Hi-Z	-- PU

REDWOOD 1 LEAKAGE CONTROL PIN STATUS (cont'd)

Group/ Plane	Pin Name	Operating State (Full-On, Doze, Sleep)		Suspend State	Remarks and Ext PU/PD Requirements
DRAM		TYPE	Idle State	Pin State	
DRM/2	MA<11:1>	I/O	X	Hi-Z	PU/PD (power on straps)
DRM/2	MA0A	I/O	X	Hi-Z	PU/PD (power on straps)
DRM/2	MA0B	I/O	X	Hi-Z	PU/PD (power on straps)
DRM/2	RAS<2:0>#	O	1	Hi-Z	--
DRM/2	CAS<3:0>A#, CAS<3:0>B#	O	1	Hi-Z	--
DRM/2	DRAMWE#	O	1	Hi-Z	--
DRM/2	MDEN#	O	1	Hi-Z	--

CLK & RESET		TYPE	Idle State	Pin State	
PM/3	CLK1X2X	I	Input	-	--
CPU/1	CPUCLKO1	O	X	Hi-Z	--
CPU/1	CPUCLKO2	O	X	Hi-Z	--
PM/3	RCRST#	I	Input	1	RCRST# is always H except when RTC Battery is dead
PM/3	PWRGOOD	I	Input	1	--
CPU/1	(RSTCPU)	O	0	Hi-Z	--
AT/1	(RSTDRV)	O	0	Hi-Z	--
CPU/1	(RSTNPU)	O	0	Hi-Z	--
AT/3	SPNDNRST	O	0	Hi-Z	--
AT/3	RSTDRV#	O	1	Hi-Z	--

AT BUS		TYPE	Idle State	Pin State	
AT/3	MASTER#	I	1	-	--
AT/3	KBCS#	O	1	Hi-Z	PU if KBC is powered-On during Suspend
AT/3	ROMCS#	O	1	Hi-Z	--
int RTC/3	(IRQ8#)	O	1	Hi-Z	--
ext ETC/3	(IRQ8#)	I	1	-	--
AT/3	(KBRST#)	I	1	-	--
GPIO/3	(GPCS0#)	O	1	Hi-Z	--
GPIO/3	(GPIOC1)	I/O	X	Hi-Z	PD if not used

REDWOOD 1 LEAKAGE CONTROL PIN STATUS (cont'd)

Group/ Plane	Pin Name	Operating State (Full-On, Doze, Sleep)		Suspend State	Remarks and Ext PU/PD Requirements
POWER MGMT		TYPE	Idle State	Pin State	
PM/3	32KIN	I	X	-	--
PC/3	PC0	O	X	Hi-Z	--
PC/3	PC1	O	X	Hi-Z	--
PC/3	PC2	O	X	Hi-Z	--
GPIO/3	(GPCS1#)	O	1	Hi-Z	--
GPIO/3	(GPIOC0)	I/O	X	Hi-Z	PD if not used
PC/3	PC3	O	X	Hi-Z	--
GPIO/3	(GPCS2#)	O	1	Hi-Z	--
PM/3	(HTRGOUT)	O	X	Hi-Z	--
PC/5	PC4	O	X	Hi-Z	--
GPIO/5	(GPCS3#)	O	1	Hi-Z	--
PM/5	(EXTACT3)	I	0	-	PD if not used
L2/5	TAGD1	I/O	X	Hi-Z	PD if Static-Suspend supported
PC/5	PC5	O	X	Hi-Z	--
LED/5	(SPLEDFLSH)	O	0	Hi-Z	--
L2/5	TAGD2	I/O	X	Hi-Z	PD if Static-Suspend supported
PC/5	PC6	O	X	Hi-Z	--
LED/5	(LBLEDFLSH)	O	X	Hi-Z	--
L2/5	TAGD3	I/O	X	Hi-Z	PD if Static-Suspend supported
PC/5	PC7	O	X	Hi-Z	--
GPIO/5	(GPIOA0)	I/O	X	Hi-Z	PD if not used
PM/5	(EXTACT2)	I	0	-	PD if not used
L2/5	TAGD4	I/O	X	Hi-Z	PD if Static-Suspend supported
PC/5	PC8	O	X	Hi-Z	--
GPIO/5	(GPIOA1)	I/O	X	Hi-Z	PD if not used
L2/5	TAGD5	I/O	X	Hi-Z	PD if Static-Suspend supported
PC/5	PC9	O	X	Hi-Z	--
L2/5	TAGD6	I/O	X	Hi-Z	PD if Static-Suspend supported
GPIO/3	GPIO0	I/O	X	Hi-Z	PD if not used
PM/3	(FRCSLW)	I	0	-	--
PM/3	(GPEXT)	O	1	Hi-Z	--
extRTC	(RWRTC)	O	0	Hi-Z	--
GPIO/3	GPIO1	I/O	X	Hi-Z	PD if not used
AT/3	(KBGA20)	I	Input	-	--
AT/3	(KBCLKO)	O	0	Hi-Z	--
extRTC	(DSRTC)	O	0	Hi-Z	--
GPIO/3	(GPIO2)	I/O	X	Hi-Z	PD if not used
PM/3	(RING)	I	0	-	PD if not used
DRM/3	(MDEN#)	O	1	0	--
extRTC	(ASRTC)	O	0	Hi-Z	--
GPIO/3	(GPIO3)	I/O	X	Hi-Z	PD if not used
PM/3	(GPCTCLK)	I	X	-	--
PM/3	(EXTACT1)	I	0	-	PD if not used
PM/3	SWTCH	I	0	0	--

REDWOOD 1 LEAKAGE CONTROL PIN STATUS (cont'd)

Group/ Plane	Pin Name	Operating State (Full-On, Doze, Sleep)		Suspend State	Remarks and Ext PU/PD Requirements
BURST BUS		TYPE	Idle State	Pin State	
BBus/4	BADS#	I/O	1	Hi-Z	PU
BBus/4	FS1XCLK	O	X	Hi-Z	--
BBus/4	BD<7:0>	I/O	X	Hi-Z	PU
BBus/4	BSER	I	1	-	--
BBus/4	BDEV#	I/O	1	Hi-Z	PU

L2 CACHE		TYPE	Idle State	Pin State	
L2/5	(TAGD0)	I/O	X	Hi-Z	PD if Static-Suspend supported
L2/5	(TAGD7)	I/O	X	Hi-Z	PD if Static-Suspend supported
	(HIT#)	I	1	-	--
L2/5	(CA3A)	O	X	Hi-Z	--
L2/5	(CA3)	O	X	Hi-Z	--
L2/5	(CA3B)	O	X	Hi-Z	--
L2/5	(CA2)	O	X	Hi-Z	--
L2/5	CWE<1:0>#	O	1	Hi-Z	PU
L2/5	(CCS0#)	O	1	Hi-Z	--
PM/5	(LB)	I	X	-	PD if not used
L2/5	(CCS1#)	O	1	Hi-Z	--
PM/5	(VLB)	I	X	-	PD if not used
L2/5	(CCS2#)	O	1	Hi-Z	--
PM/5	(ACPWR)	I	X	-	PD if not used
L2/5	(CCS3#)	O	1	Hi-Z	--
PM/5	(FBE#)	O	1	Hi-Z	--
L2/1	COE<1:0>#	O	1	Hi-Z	--
L2/5	(DIRTY)	I/O	X	Hi-Z	--
PM/5	(GPIOB0)	I/O	X	Hi-Z	PD if not used
PM/5	(WAKE0)	I	0	-	--
L2	TAGWE#	O	1	Hi-Z	--
L2	(DRTWE#)	O	1	Hi-Z	--
PM	(GPIOB1)	I/O	X	Hi-Z	PD if not used
PM	(WAKE1)	I	0	-	--
CPU	(NMI)	I	0	-	--

REDWOOD 2 LEAKAGE CONTROL PIN STATUS

Group/ Plane	Pin Name	Operating State (Full-On, Doze, Sleep)		Suspend State	Remarks and Ext PU/PD Requirements
CPU INTERFACE		TYPE	Idle State	Pin State	
CPU/1	D<31:0>	I/O	X	Off	--
CPU/1	RDY#	I/O	1	Off	PU
CPU/1	BRDY#	I	1	Off	PU
CPU/1	(DP<3:0>)	I/O	X	Off	optional PU
PM/1	(GPIO<7:4>)	I/O	X	Off	PD if not used
VL/1	(LREQ<1:0>#)	I	1	Off	PU
VL/1	(LGNT<1:0>#)	O	1	Off	PU
CPU/1	(FERR#)	I	1	Off	PU if coprocessor not available
	(W/R#)	I	X	Off	--
CPU/1	IGNNE#	O	1	Off	--
CPU/1	INTR	O	0	Off	--
CPU/1	HOLD	O	0	Off	--
CPU/1	HLDA	I	0	Off	--
CPU/1	NMI	O	0	Off	--
CPU/1	(HITM#)	I	1	Off	PU
AT/1	(IRQ13)	I	0	Off	--

VL BUS		TYPE	Idle State	Pin State	
VL/1	LOCAL#	I	1	Off	PU if not totem-pole from VL device
VL/1	LRDY#	I	1	Off	PU
VL/1	(LREQ1#)	I	1	Off	PU
VL/1	(LOCAL2#)	I	1	Off	PU if not totem-pole from VL-device
VL/1	LREQ0#	I	1	Off	PU
VL/1	(LGNT1#)	O	1	Off	PU
VL/1	(LOCAL1#)	I	1	Off	PU if not totem-pole from VL-device
VL/1	LGNT0#	O	1	Off	PU

CLK & RESET		TYPE	Idle State	Pin State	
AT/3	14MHZIN	I	X	Off	--
CPU/1	CPUCLK	I	X	Off	--
AT/3	RSTDRV#	I	1	Off	--

REDWOOD 2 LEAKAGE CONTROL PIN STATUS (cont'd)

Group/ Plane	Pin Name	Operating State (Full-On, Doze, Sleep)		Suspend State	Remarks and Ext PU/PD Requirements
AT BUS		TYPE	Idle State	Pin State	
AT/3	SA<1:0>	I/O	X	Off	--
AT/3	SHBE#	I/O	1	Off	--
AT/3	SD<7:0>	I/O	X	Off	PU
AT/3	SD<15:8>	I/O	X	Off	PU
AT/3	(MSA<7:0>)	O	X	Off	--
AT/3	BALE	O	0	Off	--
AT/3	MASTER#	I	1	Off	PU
AT/3	MEMR#	I/O	1	Off	PU
AT/3	MEMW#	I/O	1	Off	PU
AT/3	SMEMR#	O	1	Off	PU
AT/3	SMEMW#	O	1	Off	PU
AT/3	IOR#	I/O	1	Off	PU
AT/3	IOW#	I/O	1	Off	PU
AT/3	MEMCS16#	I	1	Off	PU
AT/3	IOCS16#	I	1	Off	PU
AT/3	IOCHCK#	I	1	Off	PU
AT/3	IOCHRDY	I	0	Off	PU
AT/3	ZWS#	I	1	Off	PU
AT/3	SYSCLK	O	X	Off	--
AT/3	AEN	O	0	Off	--
AT/3	TC	O	0	Off	--
AT/3	REFRESH#	I/O	1	Off	PU
AT/3	IRQ<15:14>	I	0	Off	PU
AT/3	IRQ<12:3>	I	0	Off	PU
AT/3	IRQ<1>	I	0	Off	--
AT/3	DRQ<2:0>	I	0	Off	optional PD
AT/3	DRQ<3>	I/O	0	Off	optional PD
AT/3	DRQ<7:5>	I/O	0	Off	optional PD
AT/3	DACK<3:0>#	O	1	Off	--
AT/3	DACK<7:5>#	O	1	Off	--

REDWOOD 2 LEAKAGE CONTROL PIN STATUS (cont'd)

Group/ Plane	Pin Name	Operating State (Full-On, Doze, Sleep)		Suspend State	Remarks and Ext PU/PD Requirements
BUFFER CNTL		TYPE	Idle State	Pin State	
AT/3	XDDIR	O	X	Off	--
AT/3	SAEN#	O	1	Off	--
Misc/3	(TYPE2)	I	X	Off	PU/PD (power on strap)

BURST BUS		TYPE	Idle State	Pin State	
BBus/4	BADS#	I/O	1	Off	PU
BBus/4	FS1XCLK	I	X	Off	--
BBus/4	BD<7:0>	I/O	X	Off	PU
BBus/4	BDEV#	I/O	1	Off	PU
BBus/4	BSER	O	1	Off	--
BBus/4	BINT#	I	1	Off	PU

MISC CONTROL		TYPE	Idle State	Pin State	
AT/3	(SPKR)	O	X	Off	--
Misc/3	(TSTOUT2)	O	0	Off	--
AT/3	TURBO	O	X	Off	--
PM/3	DETURBO	I/O	X	Off	--
AT/3	IDECS0#	O	1	Off	--
AT/3	IDECS1#	O	1	Off	--
AT/3	IDED7	I/O	X	Off	--
AT/3	IDEBUFEN#	O	1	Off	--

----- End of Document -----

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Redwood/FIR Application Note

Abstract : **CPU Address mapping to MA lines**
Date / Revision : **1/24/93** **Rev 1.0**

PINE	REDWOOD	FIR
—	☺ Rev 0, A0, A1	☺ Rev 0, A0, A1

☺	= Applicable
☹	= Not Applicable
—	= Function Not Available

This document describes the address multiplexing scheme on Redwood/FIR's DRAM controller for customers who need the information for asymmetric DRAM support or customization the DRAM MA interface.

INTERLEAVE ON

8-bit column address

MA	11	10	9	8	7	6	5	4	3	2	1	0
RAS	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11
CAS					A9	A8	A7	A6	A5	A4	A10	A3

9-bit column address

MA	11	10	9	8	7	6	5	4	3	2	1	0
RAS	A23	A22	A21	A19	A18	A17	A16	A15	A14	A13	A12	A20
CAS				A11	A9	A8	A7	A6	A5	A4	A10	A3

10-bit column address

MA	11	10	9	8	7	6	5	4	3	2	1	0
RAS	A24	A23	A21	A19	A18	A17	A16	A15	A14	A13	A22	A20
CAS			A12	A11	A9	A8	A7	A6	A5	A4	A10	A3

11-bit column address

MA	11	10	9	8	7	6	5	4	3	2	1	0
RAS	A25	A23	A21	A19	A18	A17	A16	A15	A14	A24	A22	A20
CAS		A13	A12	A11	A9	A8	A7	A6	A5	A4	A10	A3

12-bit column address

MA	11	10	9	8	7	6	5	4	3	2	1	0
RAS	A25	A23	A21	A19	A18	A17	A16	A15	A26	A24	A22	A20
CAS	A14	A13	A12	A11	A9	A8	A7	A6	A5	A4	A10	A3

INTERLEAVE OFF

8-bit column address

MA	11	10	9	8	7	6	5	4	3	2	1	0
RAS	A21	A20	A10	A19	A18	A17	A16	A15	A14	A13	A12	A11
CAS					A9	A8	A7	A6	A5	A4	A2	A3

9-bit column address

MA	11	10	9	8	7	6	5	4	3	2	1	0
RAS	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11
CAS				A10	A9	A8	A7	A6	A5	A4	A2	A3

10-bit column address

MA	11	10	9	8	7	6	5	4	3	2	1	0
RAS	A23	A22	A20	A19	A18	A17	A16	A15	A14	A13	A12	A21
CAS			A11	A10	A9	A8	A7	A6	A5	A4	A2	A3

11-bit column address

MA	11	10	9	8	7	6	5	4	3	2	1	0
RAS	A24	A22	A20	A19	A18	A17	A16	A15	A14	A13	A23	A21
CAS		A12	A11	A10	A9	A8	A7	A6	A5	A4	A2	A3

12-bit column address

MA	11	10	9	8	7	6	5	4	3	2	1	0
RAS	A25	A22	A20	A19	A18	A17	A16	A15	A14	A24	A23	A21
CAS	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A2	A3

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Redwood/FIR Application Note

Abstract : **Important Design Considerations of RW/FIR based systems**
Date / Revision : **1/24/93** **Rev 1.10**

Applies to :

PINE	REDWOOD	FIR
—	☺ 0, A0, A1	☺ 0, A0, A1

☺	= Applicable
☹	= Not Applicable
—	= Function Not Available

This document tries to clarify some of the signals usage and some design concept used by Redwood/FIR which may not be obvious from the databook.

VOLTAGE PLANES

Redwood/FIR1 and Redwood/FIR2 has many programmable voltage planes. Most of them are independent of each others and the chip will take care of the level translation between signal groups with different power rails. However, in the early silicons, including Rev 0 and Rev A0, the VCC_CL (core logic), VCC_ISA (Group 3) and VCC_BBUS (Group 4) are required to be the same voltage since they are not level translated internally. The Rev A1 silicon will be equipped with proper level translation cells between Core, ISA and BBus interface so that Rev A1 (and future) silicon will allows fully independent power rails.

Also, one important note about the voltage plane is, since PC0-9 are required to be driven properly during Suspend, therefore, both Group 3 and Group 5 power planes should be kept ON (in addition to VCC_CL). However, since it will not lead to any extra power consumption, we suggest all voltage planes of Redwood1/FIR1 to be powered during Suspend to simplify the power control circuit as all output signals will be properly leakage controlled.

PWRGOOD & RCRST#

If the customers has designed in PicoPower 268 or 368, they will found these two signals' functionality are very different between Evergreen family and RW/FIR chipset. Anyway, the functions of these two pins requires some explanations.

PIN	FUNCTION IN 268/PINE	FUNCTION IN RW/FIR
PWRGOOD	Enable leakage control for 206	Latches the MA strap options (when goes L->H) Wake up the chips from Off (when goes L->H) Put the chips into Off (when goes H->L) Can be used as Hardware Reset (prog. options)
RCRST#	Hardware reset the 268/PINE Latches the MA strap options	Keep the RTC CMOS content (when kept H)

In 268/PINE design, it is required to drive PWRGOOD *low during Suspend* to turn on the leakage control of 206.
In Redwood/FIR design, PWRGOOD should stay *H during Suspend*, and driven LOW only when turning the system OFF.

LEAKAGE CONTROL

The leakage control mechanism are also quite different from 268/PINE but improved and simplier to implement.
In Redwood/FIR based designs, all leakage controlled outputs are *floated during Suspend*. The custom designed I/O cells on Redwood1/FIR1 will not leak current even the signal is floating, this simplifies the leakage control considerations :

CPU LOCAL BUS :

During Suspend, CPU is off, VL-Bus of the VL-devices are off (even their core may still be powered), this will clamp virtually all signals to Low due to the input protection diode.

ISA BUS :

During Suspend, ISA bus and all devices should be powered off and therefore no leakage current. If devices like Modem and Network are still powered for Modem RING wakeup or to service Network polling, they should at least be capable of powering off on the ISA bus side so that the RING or IRQ signals from the devices will wakeup Redwood1/FIR1 through any of the four external wakeup resources, namely, WAKE0, WAKE1, RING and SWTCH.

Keyboard Controller :

Many designs keep the keyboard scanner/controller On during Suspend for special functions like battery charging function etc and the controller doesn't expect KBCS# to be Low during Suspend. In Redwood/FIR design, since the KBCS# is floated during Suspend, we can simply use a weak pullup resistor to keep it High.

DURING SUSPEND

During 5V- or 3V-Suspend (Suspend-to-RAM), the Redwood1/FIR1 should be powered-on because the PMC and all the Wakeup resources, RTC etc are inside Redwood1/FIR1 and its outputs are leakage controlled. However, Redwood2/FIR2 should be *powered-off* during Suspend. This is because Redwood2/FIR2 doesn't contain any PMC circuitry and it is mainly ISA, VL and B-Bus interfaces which are all powered off during Suspend, therefore, the leakage control mechanism is not implemented on Redwood2/FIR2.

One remark is, the 8237s, 8254, 8259s shadow registers are all located inside Redwood2/FIR2, therefore, to resume the system properly, we need to read all the shadow registers from Redwood2/FIR2 before power it off.

CLOCK OUTPUTS

For all new designs based on Rev A and future silicons, designers should notice the change in clock output definition and should always use the new definition.

Pin 153	CPUCLKO1: 12mA	This output is always 1X Clock and can be programmed to be running regardless of STOPCLK state. This is intended to be used to drive Redwood2/FIR2 and VL-CLK.
Pin 151	CPUCLKO2 : 8mA	This can be either 1X for 486 or 2X for 386 type CPU depending upon index Reg 100H Bit 1. This output should be connected to CPU Clock input.

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Redwood/FIR Application Note

Abstract : **Using the various Reset signals on Redwood / FIR**
Concept of Redwood1/FIR1 Standby state (Off)

Date / Revision : **1/20/93** **Rev 1.0**

Applies to :

PINE	REDWOOD	FIR
--	☺	☺

☺	= Applicable
☹	= Not Applicable
--	= Function Not Available

RESET SIGNALS CLARIFICATION :

	Nominal Functions
SRESET	Soft Reset : This output to SL-Enhanced CPU indicating a software generated CPU reset request. It will also be active during a hardware generated reset condition. This pin ***should be used with CPU with a single reset pin.***
RSTCPU/RSTDRV	AT/CPU Reset : This output is used to reset AT bus devices. In case of SL-Enhanced CPU, this pin is also connected to the RSTCPU pin of the CPU (hardware reset).
RSTDRV#	AT Bus Reset Output# : This provides an active *low* reset signals to devices like KB controller, VL-Bus, IDE drives etc. It is exactly the same timing as RSTDRV pin except the polarity is inverted.
SPNDNRST	Suspend Not Reset : This output provides a reset equivalent to RSTDRV except it will not toggle (L->H->L) during Resume. Any device not powered off during Suspend Mode should use this reset pin.

CONCEPT OF REDWOOD1/FIR1 STANDBY STATE

There are a lot of terminology problems since every vendor and manufacturer have their own definitions of states like Standby. This document tries to clarify what is Standby state in Redwood/FIR based design.

Redwood1/FIR1, due to the internal RTC, must be powered all the time, either by Main Battery, AC power or RTC Backup battery, because the chip is always powered, instead of OFF state, we call it STANDBY state and it can be used interchangeably with OFF.

Since the RTC is powered by the VCC_CL plane, which also powers all the high speed logic, the chip should be waken up only when the DC/DC converter or AC power is stabilized, otherwise, the chip will drain high current from the RTC battery. The best indicator of DC/DC converter or AC power stable is PWRGOOD, therefore, PWRGOOD is used to wakeup the chip from Standby state to Fully-On state.

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For the same reason, when PWRGOOD toggles to Low, it indicates that DC/DC converter or AC power is Off, so that PWRGOOD will logically put the Redwood1/FIR1 to Standby State in order not to drain excessive current from RTC Battery and this is also the Off state of the chip.

During Suspend, since the DC/DC converter should still be powering the Redwood1/FIR1, DRAM (optional VGA controller and video RAM), therefore, PWRGOOD should stay High to avoid driving Redwood1/FIR1 to Standby state.

Summarizing, PWRGOOD is the signal differentiating between Suspend and Standby (Off) in Redwood/FIR based design.

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